AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Autonomous)

(Approved by A.I.C.T.E., New Delhi & Permanently Affiliated to JNTU-GV, Vizianagaram)
NAAC Accredited with A+ grade
Tamaram (V), Makavarapalem, Narsipatnam (RD), Anakapalle Dist, Pin-531113

DEPARTMENT OF ECE- ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC REGULATIONS

COURSE STRUCTURE AND SYLLABUS

For PG-R24

M.Tech – VLSI Design

(Applicable for batches admitted from 2024-2025)

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www.avanthienggcollege.ac.in, mail: principal@avanthienggcollege.ac.in

Academic Regulations (R24) for M.Tech (Regular) Degree Course

(Applicable for the students of M.Tech from the Academic Year 2024-2025 onwards)

1. ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the Institute from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the Institute or on the basis of any other order of merit as approved by the Institute, subject to reservations as laid down by the Govt. from time to time.

2. AWARD OF M. Tech DEGREE

a) A student shall be declared eligible for the award of the M.Tech Degree, if he pursues a course of study in not less than two and not more than four academic years.

b) The student shall register for all 68 credits and secure all the 68 credits.

c) The minimum instruction days in each semester are 90.

3. PROGRAMME OF STUDY

The following specializations are offered at present for the M.Tech Programme of study.

M.Tech

1. M.Tech- Computer Science & Engineering
2. M.Tech- Power Systems
3. M.Tech- Power Electronics
4. M.Tech- Digital Electronics and Communication Systems
5. M.Tech- VLSI Design

And any other course as approved by AICTE/University from time to time.

4. Departments offering M. Tech Programmes with specializations are noted below:

Department	Programme Code	Title
EEE	56	M.Tech- Power Systems

EEE	43	M.Tech- Power Electronics
ECE	38	M.Tech- Digital Electronics and Communication Systems
ECE	72	M.Tech - VLSI Design
CSE	58	M.Tech - Computer Science & Engineering

5. ATTENDANCE

a) A student shall be eligible to write the examinations of the institute if he acquires a minimum of 75% of attendance in aggregate of all the subjects / courses, and with minimum 50% in each and every course including practicals.

b) Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

c) Shortage of Attendance **below** 65% in aggregate shall not be condoned and not eligible to write their end semester examination of that class.

d) Students whose shortage of attendance is not condoned in any semester are not eligibleto write their end semester examination of that class.

e) A prescribed fee shall be payable towards condonation of shortage of attendance.

f) A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek re-admission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for re-admission into the same class.

6. EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practical, on the basis of InternalEvaluation and End Semester Examination.

a) For the theory subjects 75 marks shall be awarded based on the performance in the End Semester Examination and 25 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each midterm examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks, and it will be reduced to 25 marks. End semester examination is conducted for 75 marks for all FIVE (5) questions (one question from one unit) to be answered (either or).

b) For practical subjects, 75 marks shall be awarded based on the performance in the End Semester Examinations and 25 marks shall be awarded based on the day-to-day performance as Internal Marks. The internal evaluation based on the day to day work-5 marks, record- 5 marks and the remaining 15 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup mark of Procedure-20, Experimentation-30, Results-10, and Viva-voce-15.

c) For Mini Project with Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor / mentor and two other senior faculty members of the department. For Mini Project with Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

d) A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

e) In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to re-appear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided, the internal marks secured by a candidate are less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt shall stand cancelled. For re-registration, the candidates have to apply to the college by paying the requisite fees and get approval from the institute before the start of the semester in which re-registration is required.

f) In case the candidate secures less than the required attendance in any re-registered subject(s), he shall not be permitted to write the End Examination in that subject. He shall again re-register the subject when next offered.

g) Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher or teacher of the respective college and the

second examiner shall be appointed by the institute from the panel of examiners submitted by the respective departments.

7. EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

a) A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members in the department.

b) Registration of Dissertation/ Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

c) After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

d) If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the PRC shall examine whether or not to change the topic/supervisor leads to a major change in initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

e) Continuous assessment of Dissertation-I and Dissertation-II during the Semester(s) will be monitored by the PRC.

f) A candidate shall submit his status report in two stages to the PRC, at least with a gap of 3 months between them.

g) The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

h) Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

i) The thesis shall be adjudicated by one examiner selected by the institute. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

j) If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is

unfavorable again, the thesis shall be summarily rejected. The candidates have to re-registered for the project and complete the project within the stipulated time after taking the approval from the Institute.

k) The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination.

l) If the report of the examiner is favorable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work for a maximum of 100 marks as one of the following:

I. Excellent
II. Good
III. Satisfactory
IV. Unsatisfactory

m) If the report of the Viva-Voce is unsatisfactory (ie, < 50 marks), the candidate shall retake the Viva- Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the college.

8. Cumulative Grade Point Average (CGPA)

As measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed: **A**fter each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Marks Range Theory/ Laboratory (Max – 100)	Marks Range Mini Project/ Project Work or Dissertation (Max – 100)	Letter Grade	Level	Grade Point
≥ 90	≥ 90	S	Superior	10
≥80 to <90	≥80 to <90	A	Excellent	9
≥70 to <80	≥70 to <80	B	Very Good	8
≥60 to <70	≥60 to <70	C	Good	7
≥50 to <60	≥50 to <60	D	Average	6
<50	<50	F	Fail	0
		AB	Absent	0

i) A student obtaining Grade "F" or Grade "Ab" in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.

ii) For non-credit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/ CGPA / Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

SGPA: The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses under gone by a student, i.e.,

$$\mathbf{SGPA=\Sigma (C_i \times G_i) / \Sigma C_i}$$

Where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

CGPA: The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses under gone by a student over all the semesters of a program, i.e.

$$\mathbf{CGPA=\Sigma (C_i \times S_i) / \Sigma C_i}$$

Where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.

Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts. While computing the SGPA the subjects in whom the student is awarded Zero grade points will also be included.

Equivalent Percentage = (CGPA-0.75)*10

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale. Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by the letters S, A, B, C, D and F.

9. AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	CGPA to be secured	
First Class with Distinction	**≥ 7.75 (Without any supplementary appearance)**	**From the CGPA secured from 68 Credits.**
First Class	**≥ 7.75 (With any supplementary appearance)** **≥ 6.75 and < 7.75 (Without any**	

	supplementary appearance)	
Second Class	**≥ 6.75 and < 7.75 (With any supplementary appearance)** **≥ 6.0 to < 6.75 (Without any supplementary appearance)**	
Pass Class	**≥ 6.0 to < 6.75 (With any supplementary appearance)**	

The Grades secured, Grade points and Credits obtained will be shown separately in the memorandum of marks.

10. WITH HOLDING OF RESULTS

If the student is involved in indiscipline/malpractices/court cases, the result of the student will be withheld.

11. TRANSITORY REGULATIONS (For R24)

a) Discontinued or detained candidates are eligible for re-admission into same or equivalent subjects at a time as and when offered.

b) The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per R19 (JNTUK) academic regulations.

12. GENERAL

a) Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

b) The academic regulation should be read as a whole for the purpose of any interpretation.

c) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal / Dean-Academics of the institution is final.

d) The Institute may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institute.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

S.No	Nature of Malpractices / Improper conduct	Punishment
	If the candidate:	
1	(a) Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of anoutsider, he will be handed over

	of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination) (b) Gives assistance or guidance or receivesit from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	to the police anda case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all External examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional	Expulsion from the examination hall and

	sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all External examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in lettersto the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6	Refuses to obey the orders of the Chief Superintendent/Assistant–Superintendent/ any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work

		and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all External examinations. The continuation of the course by the candidate is subject to the Academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.

12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Institute for further action to award suitable punishment	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions : (if the squad reports that the college is also involved in encouraging malpractices)
   - (i) A show cause notice shall be issued to the college.
   - (ii) Impose a suitable fine on the college.
   - (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

Seminar/ comprehensive vivo evaluation

There shall be two seminar presentations during III semester and IV semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

(a) For Ist & IInd semesters Seminar 100 marks are allotted for each, which shall be awarded based on the performance of the student on the selected advanced topic which is subdivided as follows.

Marks for assignment	-	20
Marks for Power Point Presentation	-	60
Marks for viva voce (Orals)	-	20
Total marks	-	100

(b) There shall be two seminar presentations during III semester and IV semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee (PRC) consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

(Dr. R Prasad Rao)
Dean(Academics) &
Member Secretary (AC)

(Dr.C P V N J Mohan Rao)
Chairman
Academic Council

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Department of ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M.Tech- VLSI Design **Regulation: R24**

I Year I Semester- Course Structure

S.No	Category	Course Code	Course Title	Hours per Week			
				L	T	P	Credits
1	PC	2472PC01	CMOS Analog IC Design	3	0	0	3
2	PC	2472PC02	CMOS Digital IC Design	3	0	0	3
3	PE	2472PE01.1 2472PE01.2 2472PE01.3	**Professional Elective-1** 1. VLSI Technology 2. Nanomaterials and Nanotechnology 3. MEMS Technology	3	0	0	3
4	PE	2472PE02.1 2472PE02.2 2472PE02.3	**Professional Elective-2** 1. Device Modeling 2. Nano-electronics 3. Photonics	3	0	0	3
5	PC	2472PC03	CMOS Analog IC Design Lab	0	0	4	2
6	PC	2472PC04	CMOS Digital IC Design Lab	0	0	4	2
7	MC	24MTMC01	Research methodology and IPR	2	0	0	2
8	AC	24MTAC01.1 24MTAC01.2	**Audit Course-1** 1. English for Research paper writing 2. Disaster Management	2	0	0	0
			Total	16	0	8	18

Category	Courses	Credits
PC- Professional Core Course	4	10
PE- Professional Elective	2	6
MC-Mandatory Course	1	2
AC- Audit Course	1	0
Total	**8**	**18**

Department of ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M.Tech- VLSI Design **Regulation: R24**

I Year II Semester- Course Structure

S.No	Category	Course Code	Course Title	Hours per Week			
				L	T	P	Credits
1	PC	2472PC05	Mixed Signal & RF IC Design	3	0	0	3
2	PC	2472PC06	Physical Design Automation	3	0	0	3
3	PE	2472PE03.1 2472PE03.2 2472PE03.3	**Professional Elective-3** 1. Design For Testability 2. IOT & its Applications 3. VLSI Signal Processing	3	0	0	3
4	PE	2472PE04.1 2472PE04.2 2472PE04.3	**Professional Elective-4** 1. Network Security & Cryptography 2. Microcontrollers & programmable Digital Signal Processors 3. Low Power VLSI Design	3	0	0	3
5	PC	2472PC07	Mixed Signal IC Design Lab	0	0	4	2
6	PC	2472PC08	Physical Design Automation Lab	0	0	4	2
7	PR	2472PR01	Mini Project	0	0	4	2
8	AC	2472AC02.1 2472AC02.2	**Audit Course – 2** 1. Constitution of India 2. Value Education	2	0	0	0
			Total	14	0	12	18

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

Category	Courses	Credits
PC- Professional Core Course	4	10
PE- Professional Elective	2	6
PR-Mini Project	1	2
AC- Audit Course	1	0
Total	**8**	**18**

CMOS Analog IC Design

Course Title: CMOS Analog IC Design	I Year- I Semester
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PC01
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre-requisites: Fundamentals of Electronics, Linear Circuit Analysis, Digital Logic Design, Semiconductor Physics, Signal Processing Fundamentals.	

Course objectives:

- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- Intuitive understanding and real-life applications are emphasized throughout the course.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two- Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
- To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

Course Outcomes:

At the end of the course, students will be able to:

CO1	Design MOSFET based analog integrated circuits.
CO2	Analyze analog circuits at least to the first order.
CO3	Appreciate the trade-offs involved in analog integrated circuit design.
CO4	Understand and appreciate the importance of noise and distortion in analog circuits.
CO5	Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
CO6	Solve engineering problems for feasible and optimal solutions in the core area of analog ICs.

UNIT -I

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT -II:

Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors– Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.

UNIT -III:

Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT -IV:

Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation.

UNIT -V:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Text Books:

1. Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition2016.
2. Paul. R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.

Reference Books:

1. T. C. Carusone, D. A. Johns & K. Martin, "Analog Integrated Circuit Design", 2nd Edition,Wiley, 2012.
2. P.E.Allen&D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.
4. Recent literature in Analog IC Design.

Web References:

1. https://electrovolt.ir/wp-content/uploads/2014/08/Design-of-Analog-CMOS-Integrated-Circuit-2nd-Edition-ElectroVolt.ir_.pdf
2. https://archive.nptel.ac.in/courses/117/101/117101105/

CMOS Digital IC design

Course Title: CMOS Digital IC design	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PC02
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Basic Electronics, Semiconductor Physics, Digital Logic Design, Circuit Analysis, VLSI Design Fundamentals.	

Course objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits, and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes:

At the end of the course, students will be able to:

CO1	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.
CO2	Classify different semiconductor memories.
CO3	Analyze, design and implement combinational and sequential MOS logic circuits.
CO4	Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
CO5	Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

UNIT-I: MOS Design

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, output high voltage, Output Low voltage, gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II: Combinational MOS Logic Circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OAI gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III: Sequential MOS Logic Circuits

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV: Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V: Semiconductor Memories

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Text Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan Borivoje Nikolic, 2nd Ed., PHI.

Web References:

1. https://rajeev2007.github.io/VLSI/0072460539cmos.pdf
2. https://onlinecourses.nptel.ac.in/noc21_ee09/preview
3. https://www.udemy.com/course/cmos-digital-integrated-circuit_design/?srsltid=AfmBOopyWeqE_jTRGy2hw4zcUhI_7_lutT_bOlTrRmUqpPJ_2ruTXNq&couponCode=NVDIN35

VLSI Technology
(Elective I)

Course Title: VLSI Technology (Elective I)	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE01.1
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Digital Electronics, Semiconductor Physics, Circuit Theory, Microelectronics, MOSFET Basics.	

Course Objectives:

- Gain a solid foundation in VLSI design principles and methodologies for digital and analog circuits.
- Develop proficiency in industry-standard tools for design, simulation, and verification.
- Explore power optimization techniques and the semiconductor manufacturing process.
- Engage in innovative research and enhance collaboration and communication skills in VLSI projects.

Course Outcomes

At the end of the course the student able to

CO1	Understand the basics of MOS transistors and also the characteristics of MOS transistors.
CO2	Learn about the MOS fabrication process and short channel effects.
CO3	Learn about the basic rules in layout designing.
CO4	Analyze various combinational logic networks and sequential systems.

UNIT 1: MOS Transistors

Introduction, The Structure of MOS Transistors, The Fluid Model, The MOS Capacitor, The MOS Transistor, Modes of Operation of MOS Transistors, Electrical Characteristics of MOS Transistors, Threshold Voltage, Transistor Trans conductance gm, Figure of Merit, Body Effect, Channel-Length Modulation, MOS Transistors as a Switch, Transmission Gate.

UNIT 2: MOS Fabrication Technology

Introduction, Basic Fabrication Processes, Wafer Fabrication, Oxidation, Mask Generation, Photolithography, Diffusion, Deposition. N-MOS Fabrication Steps, CMOS Fabrication Steps, n-Well Process, p-Well Process, Twin-Tub Process, Latch-Up Problem and Its Prevention, Use of Guard Rings, Use of Trenches, Short-Channel Effects-Channel Length Modulation Effect. Drain-Induced Barrier Lowering, Channel Punch Through, Hot carrier effect, Velocity Saturation Effect.

UNIT 3: Layout Design Rules

Scaling Theory, Scalable CMOS Design Rules, CMOS Process Enhancements, Transistors, Interconnects, Circuit Elements, Efficient layout Design techniques.

UNIT 4: Combinational Logic Networks

Layouts for logic networks. Delay through networks. Power optimization. Switch logic networks. Combinational logic testing.

UNIT 5: Sequential Systems

Memory cells and Arrays, clocking disciplines, sequential circuit Design, Performance Analysis, Power optimization, Design validation and testing.

Text Books:

1. Principals of CMOS VLSI Design-N.H.EWeste, K. Eshraghian, 2nd Edition, Addison Wesley.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.
3. Low-Power VLSI Circuits and Systems,Ajit Pal, SPRINGER PUBLISHERS
4. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Reference Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

Web References:

1. https://www.vlsitechnologyllc.com/
2. https://archive.nptel.ac.in/courses/117/106/117106093/

NANOMATERIALS AND NANOTECHNOLOGY
(Elective I)

Course Title: NANOMATERIALS AND NANOTECHNOLOGY (Elective I)	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE01.2
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Material Science, Quantum Mechanics, Solid State Physics, Thermodynamics, Surface Chemistry.	

Course Objectives:

- Acquire a comprehensive understanding of nanomaterials, their properties, and synthesis methods.
- Explore applications of nanotechnology across various fields, including electronics, medicine, and energy.
- Develop skills in characterization techniques for analyzing nanomaterials at the nanoscale.
- Engage in research projects to innovate and apply nanotechnology solutions to real-world challenges.

Course Outcomes:

At the end of the course, students will be able to:

CO1	To understand the basic science behind the design and fabrication of nano scale systems.
CO2	To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
CO3	To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
CO4	To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT I

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT II

Fundamentals of nano materials, Classification, Zero-dimensional nano materials, One-dimensional nano materials, Two-dimensional nano materials, Three dimensional nano materials. Low- Dimensional Nano materials and its Applications, Synthesis, Properties, and Applications of Low- Dimensional Carbon-Related Nano materials.

UNIT III

Micro- and Nanolithography Techniques, Emerging Applications Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication

Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT IV

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - multi-walled nano tubes, Single-walled nano tubes Optical properties of CNT‟s, Electrical transport in perfect nano tubes, Applications as case studies. Synthesis and Applications of CNT's.

UNIT V

Ferroelectric materials, coating, molecular electronics and nano electronics, biological and environmental, membrane based application, polymer based application.

Text Books:

1. Kenneth J. Klabunde and Ryan M. Richards, “Nanoscale Materials in Chemistry”, 2nd edition, John Wiley and Sons, 2009.
2. I Gusev and A ARempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGraw Hill Education 2012.

Reference Books:

1. Bharat Bhushan, “Springer Handbook of Nanotechnology”, Springer, 3rd edition, 2010.
2. Kamal K. Kar, “Carbon Nanotubes: Synthesis, Characterization and Applications”, Research Publishing Services; 1 st edition, 2011, ISBN-13: 978-9810863975.

Web References:

1. https://onlinelibrary.wiley.com/journal/nax
2. https://nptel.ac.in/courses/118104008
3. https://archive.nptel.ac.in/courses/113/106/113106093/

MEMS Technology (Elective I)

Course Title: MEMS Technology (Elective I)	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE01.3
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Material Science, Microfabrication Techniques, Solid-State Physics, Electronics Fundamentals, Mechanical Engineering Basics.	

Course Objectives:

- Understand the principles and applications of micro-electromechanical systems (MEMS) technology.
- Explore fabrication techniques, including lithography and etching processes.
- Develop design skills using simulation tools for MEMS devices.
- Investigate diverse applications of MEMS in sensors, actuators, and biomedical fields.

Course Outcomes:

At the end of the course, students will be able to:

CO1	To understand the basic concepts of MEMS technology and working of MEMS devices.
CO2	To understand and selecting different materials for current MEMS devices and competing Technologies for future applications
CO3	To understanding the concepts of fabrication process of MEMS, Design and Packaging Methodology.
CO4	To analyze the various fabrication techniques in the manufacturing of MEMS Devices.

UNIT-I: Introduction to MEMS

Introduction to MEMS & Real world Sensor/Actuator examples (DMD, Air-bag, pressure sensors). MEMS Sensors in Internet of Things (IoT), Bio-Medical Applications

UNIT-II: MEMS Materials and Their Properties

Materials (e.g. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson‟s ratio, density, piezo-resistive coefficients, TCR, Thermal Conductivity, Material Structure. Understanding Selection of materials based on applications.

UNIT-III: MEMS Fab Processes – 1

Understanding MEMS Processes & Process parameters for: Cleaning, Growth &Deposition, Ion Implantation & Diffusion, Annealing, Lithography. Understanding selection of Fab processes based on Applications.

UNIT-IV: MEMS Fab Processes – 2

Understanding MEMS Processes & Process parameters for: Wet & Dry etching, Bulk& Surface Micromachining, Die, Wire & Wafer Bonding, Dicing, Packaging. Understanding selection of Fab processes based on Applications

UNIT-V: MEMS Devices

Architecture, working and basic quantitative behavior of Cantilevers, Micro heaters, Accelerometers, Pressure Sensors, Micro mirrors in DMD, Inkjet printer-head. Understanding steps involved in Fabricating above devices.

Text Books:

1. An Introduction to Micro electromechanical Systems Engineering; 2nd Ed - by N.Maluf, K Williams; Publisher: Artech House Inc
2. Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design - by S. Senturia; Publisher: Springer

Reference Books:

1. Analysis and Design Principles of MEMS Devices - MinhangBao; Publisher:Elsevier Science.
2. Fundamentals of Micro fabrication - by M. Madou; Publisher: CRC Press; 2 editions
3. Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press
4. Micro machined Transducers Sourcebook - by G. Kovacs; Publisher: McGraw-Hill

Web References:

1. https://www.st.com/content/st_com/en/about/innovation---technology/mems.html
2. https://nptel.ac.in/courses/117105082

Device Modelling
(Elective II)

Course Title: Device Modelling (Elective II)	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE02.1
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Semiconductor Physics, Quantum Mechanics, Solid-State Electronics, Electromagnetics, Circuit Theory.	

Course Objectives:

- The principles of device physics and the mathematical foundations of device modeling.
- Learn various modeling techniques for semiconductor devices, including analytical and numerical methods.
- Gain proficiency in using simulation software to analyze and predict device behavior.
- Apply modeling concepts to real-world scenarios, enhancing skills in device design and optimization.

Course Outcomes:

At the end of the course, students will be able to:

CO1	To understand the physics of 2-terminal MOS operation and its characteristics
CO2	To understand the physics of 4-terminal MOSFET operation and its characteristics
CO3	To analyze the SOI MOSFET electrical characteristics

UNIT I

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT II

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT III

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT IV

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer‟smodel)

UNIT V

SOI MOSFET: basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

Text Books:

1. D.G.Ong , “Modern MOS Technology: Processes, Devices and Design”, McGraw Hill,1984.
2. Y.Taur and T.H.Ning, “Fundamentals of modern VLSI Devices” Cambridge Univ. Press,1998.
3. S.M.Sze, “Physics of Semiconductor Devices” Wiley,1981.

Web References:

1. **https://www.keysight.com/blogs/en/tech/educ/2024/device-modeling**
2. **https://www.sciencedirect.com/science/article/abs/pii/B9780592000428500081**
3. **https://archive.nptel.ac.in/courses/117/106/117106033/**

Nano-electronics
(Elective II)

Course Title: Nano-electronics (Elective II)	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE02.2
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Semiconductor Physics, Quantum Mechanics, Solid-State Electronics, Nanofabrication Techniques, Material Science	

Course Objectives:

- Gain a solid understanding of nano-electronic devices and their principles of operation.
- Explore fabrication techniques and materials used in nano-electronics.
- Analyze the performance and limitations of nano-scale electronic components.
- Investigate current trends and future applications of nano-electronics in various fields

Course Outcomes:

At the end of the course, students will be able to:

CO1	To understand and challenges due to scaling on CMOS devices
CO2	To analyze and explain working of novel MOS based silicon devices and various multi gate devices.
CO3	To understand working of spin electronic devices
CO4	To understand nano-electronic systems and building blocks such as: low dimensional semiconductors, heterostructures, carbon nanotubes, quantum dots, nano wires etc.

UNIT I

Properties of Individual Nanoparticles: Introduction, Metal Nano Clusters, Semiconducting Nanoparticles, Rare Gas and Molecular Clusters, Methods of Synthesis.

UNIT II

The nanoscale MOSFET, FinFETs, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.), Resonant Tunnelling Transistors.

Carbon Nanostructures: Introduction, Carbon Molecules, Carbon Clusters, Carbon Nano Tubes, Application of Carbon Nanotubes.

UNIT III

Carbon Nanotubes for Data Processing – Introduction, Electronic Properties, Synthesis of Carbon Nanotubes, Carbon Nanotube Interconnects, Carbon Nanotubes Field Effect Transistors (CNTFETs), Nanotubes for Memory Applications, Prospects of an All-CNT Nanoelectronics.

Neuroelectronic Interfacing: Semiconductor Chips with Ion Channels, Nerve Cells, and Brain: Introduction, Iono-Electronic Interface, Neuron-Silicon Circuits, Brain-Silicon Chips.

UNIT IV

Optical 3-D Time-of-Flight Imaging System: Introduction, Taxonomy of Optical 3-D Techniques, CMOS Imaging, CMOS 3-D Time-of-Flight Image Sensor, Application Examples

Pyroelectric Detector Arrays for IR Imaging: Introduction, Operation Principle of Pyroelectric IR Detectors, Pyroelectric Materials, Realized Devices, Characterization, and Processing Issues

UNIT V

Electronic Noses: Introduction, Operating Principles of Gas Sensor Elements, Electronic Noses, Signal Evaluation, Dedicated Examples. 2-D Tactile Sensors and Tactile Sensor Arrays: Introduction, Definitions and Classifications, Resistive Touch screens, Ultrasonic Touch screens, Robot Tactile Sensors, Fingerprint Sensors

Text Books:

1. Introduction to Nanotechnology, C.P. Poole Jr., F.J. Owens, Wiley (2003),
2. Nano electronics and Information Technology (Advanced Electronic Materials and Novel Devices), WaserRanier ,Wiley-VCH,2003.

Reference Books:

1. Nanosystems, K.E. Drexler,Wiley (1992).
2. The Physics of Low-Dimensional Semiconductors, John H. Davies, “Cambridge University Press, "1998

Web References:

1. https://www.sciencedirect.com/topics/engineering/nanoelectronics
2. https://nptel.ac.in/courses/117108047

PHOTONICS
(Elective II)

Course Title: PHOTONICS (Elective II)	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE02.3
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Optics, Electromagnetism, Quantum Mechanics, Material Science, Signal Processing.	

Course Objectives:

- Understand the fundamental principles of photonics and light-matter interaction.
- Explore the design and applications of photonic devices, such as lasers, sensors, and optical fibers.
- Develop skills in modeling and simulating photonic systems using relevant software tools.
- Investigate emerging trends and technologies in the field of photonics, including integrated optics and quantum photonics

Course Outcomes:

At the end of the course, students will be able to:

CO1	Classify the Optical sources and detectors and to discuss their principle.
CO2	Familiar with Design considerations of fiber optic systems.
CO3	To perform characteristics of optical fiber, sources and detectors, design as well as conduct experiments in software and hardware, analyze the results to provide valid conclusions.
CO4	apply the principles of atomic physics to materials used in optics and photonics;
CO5	calculate properties of and design modern optical fibres and photonic crystals;
CO6	use the tools, methodologies, language and conventions of physics to test and communicate ideas and explanations;
CO7	integrate several components of the course in the context of a new situation (unique to postgraduate coursework).

UNIT - I: Laser systems

General description, Laser structure, Single mode laser theory, Excitation mechanism and working of: CO2, Nitrogen, Argon ion, Excimer, X-ray, Free-electron, Dye, Nd:YAG,Alexanderite and Ti:sapphire lasers, Diode pumped solid state laser, Optical parametric oscillator (OPO) lasers. Optical amplifiers- Semiconductor optical amplifiers, Erbium doped waveguide optical amplifiers, Raman amplifiers, Fiber Lasers. Laser Applications-Lasers in Isotope separation, Laser interferometry and speckle metrology, Velocity measurements.

UNIT - II: Properties of laser Radiation

Introduction, Laser linewidth, Laser frequency stabilization, Beam divergence, Beam coherence, Brightness, focusing properties of laser radiation, Q-switching, Methods of Q- switching: Rotating- mirror method, Electro-optic Q-switching, Acoustic-optic Q-switching and Passive Q-switching, Mode locking, Methods of mode locking: Active and passive mode locking techniques, Frequency doubling and Phase conjugation

UNIT - III: Opto-electronic Devices -I

Introduction, P-N junction diode, Carrier recombination and diffusion in P-N junction, Injection efficiency, Internal quantum efficiency, Hetero-junction, Double hetero-junction, Quantum well, Quantum dot and Super lattices; LED materials, Device configuration and efficiency.

UNIT - IV: Opto-electronic Devices -II

Light extraction from LEDs, LED structures-single heterostructures, double heterostructures, Device performances and applications, Quantum well lasers; Photodiode and Avalanche photodiodes (APDs), Laser Diodes-Amplification, Feedback and oscillation, Power and efficiency, Spectral and spatial characteristics.

UNIT – V: Modulation of Light

Introduction, Birefringence, Electro-optic effect, Pockels and Kerr effects, Electro- optic Phase modulation, Electro-optic amplitude modulation, Electro-optic modulators: scanning and switching, Acousto-optic effect, Acousto-optic modulation, Raman-Nath and Bragg modulators: deflectors and spectrum analyzer, Magneto-optic effect, Faraday rotator as an optical isolator. Advantages of optical modulation.

Text books:

1. Lasers: Principles and applications by J.WilsonAndJ.F.B.Hawkes, Prentice, Hall of India, New Delhi, 1996.
2. Laser fundamentals, W.T.Silfvast, Foundation books, New Delhi, 1999.
3. Semiconductor opto electronics devices, P. Bhattacharya, Prentice – Hall of India, New Delhi, 1995.17

Reference Books:

1. Optical fiber communications, John M. Senior, Prentice-Hall of India, New Delhi, 2001
2. Optoelectronics: An Introduction, J.WilsonAndJ.F.B.Hawkes, Prentice-Hall of India, New Delhi, 1996.
3. Electro-Optical devices, M.A. Karim, Boston, Pws-Kent Publishers, 1990

Web References:

1. https://www.sciencedirect.com/topics/physics-and-astronomy/photonics
2. https://onlinecourses.nptel.ac.in/noc21_ee87/preview

Research Methodology and IPR

Course Title: Research Methodology and IPR	**I Year- I Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472MTMC01
Type of Course: Lecture	Credits: 2
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Understanding of Research Design, Familiarity with Statistical Methods, Knowledge of Intellectual Property Rights, Ability to Conduct Literature Reviews, Skills in Data Collection and Analysis.	

Course Objectives:

- Understand the principles of research methodology, including research design, data collection, and analysis techniques.
- Develop skills in formulating research questions and hypotheses relevant to scientific inquiry.
- Explore the concepts of intellectual property rights (IPR) and their significance in research and innovation.
- Learn how to protect and manage intellectual property, including patents, copyrights, and trademarks.

Course Outcomes:

At the end of this course, students will be able to

CO1	Understand research problem formulation.
CO2	Analyze research related information
CO3	Follow research ethics
CO4	Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
CO5	Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
CO6	Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT 1:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT 2:

Effective literature studies approaches, analysis Plagiarism, Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT 3:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International

Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT 4:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT 5:

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students""
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.

Reference Books:

1. Mayall , "Industrial Design", McGraw Hill, 1992.
2. Niebel , "Product Design", McGraw Hill, 1974.
3. Asimov , "Introduction to Design", Prentice Hall, 1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New
5. Technological Age", 2016.
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

CMOS Analog IC Design Lab

Course Title: CMOS Analog IC Design Lab	**I Year- I Semester**
Teaching Scheme (L:T:P): 0:0:3	Course Code: 2472PC03
Type of Course: Practical	Credits: 2
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: CMOS Technology Fundamentals, Analog Circuit Theory, Device Physics, Signal Processing Principles, Circuit Simulation Techniques.	

Course objectives

- Gain hands-on experience in designing and simulating CMOS analog integrated circuits using industry-standard tools.
- Understand the principles of analog circuit design, including operational amplifiers, filters, and voltage regulators.
- Develop skills in layout techniques and fabrication considerations for CMOS technology.
- Analyze and evaluate the performance of designed circuits through practical testing and measurement

Course Outcomes:

CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools
CO2	Grasp the significance of various cmos analog circuits in full-custom IC Design flow
CO3	Have the ability to explain the Physical Verification in Layout Design
CO4	Fully Appreciate the design and analyze of analog and mixed signal simulation
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation
CO6	The students are required to design and implement any TEN Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software.
CO7	The students are required to implement LAYOUTS of any SIX Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software. and compare the results with Pre-Layout Simulation.

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

CMOS Digital IC design Lab

Course Title: CMOS Digital IC design Lab	**I Year- I Semester**
Teaching Scheme (L:T:P): 0:0:3	Course Code: 2472PC04
Type of Course: Practical	Credits: 2
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: CMOS Technology Fundamentals, Digital Logic Design, Semiconductor Physics, Electronic Circuit Analysis, VLSI Design Principles.	

Course objectives

- Acquire practical skills in designing and simulating CMOS digital integrated circuits using professional design tools.
- Understand the principles of digital circuit design, including logic gates, flip-flops, and combinational and sequential circuits.
- Develop proficiency in layout design and verification techniques specific to CMOS technology.
- Analyze the functionality and performance of digital circuits through testing and validation in a laboratory setting.

Course Outcomes:

CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools
CO2	Grasp the significance of various design logic Circuits in full-custom IC Design.
CO3	Have the ability to explain the Physical Verification in Layout Extraction
CO4	Fully Appreciate the design and analyze of CMOS Digital Circuits
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation
CO6	The students are required to design and implement the Circuit and Layout of any TEN Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software.

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

ENGLISH FOR RESEARCH PAPER WRITING

Course Title: English for Research paper writing	**I Year- I Semester**
Teaching Scheme (L:T:P): 2:0:0	Course Code: 2472AC01.1
Type of Course: Lecture	Credits: 0
Continuous Internal Evaluation: 0 Marks	Semester End Exam: 0 Marks
Pre-requisites: Understanding academic writing conventions, familiarity with research methodologies, proficiency in grammar and vocabulary, knowledge of citation styles, awareness of ethical considerations in research.	

Course objectives:

Students will be able to:

- Understand that how to improve your writing skills and level of readability Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Course Outcomes:

CO1	Demonstrate effective planning and preparation techniques for academic writing, including structuring paragraphs and sentences clearly.
CO2	Apply strategies for clarifying ideas, avoiding ambiguity, and ensuring conciseness in written communication.
CO3	Develop skills to construct well-organized sections of a paper, including abstracts, introductions, and literature reviews.
CO4	Evaluate and critique various sections of academic papers, focusing on the methods, results, and discussion.
CO5	Utilize key skills to enhance the quality of writing in academic submissions, ensuring clarity and adherence to academic standards

Unit-1

Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit-2

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

Unit-3

Review of the Literature, Methods, Results, Discussion,Conclusions, The Final Check.

Unit-4

key skills are needed when writing a Title, key skills are neededwhen writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Unit -5

skills are needed when writing the Methods, skills needed whenwriting the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions, useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

Reference Books:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on GoogleBooks)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM.Highman‟sbook .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York DordrechtHeidelberg London, 2011.

DISASTER MANAGEMENT

Course Title: Disaster Management	**I Year- I Semester**
Teaching Scheme (L:T:P): 2:0:0	Course Code: 2472AC01.2
Type of Course: Lecture	Credits: 0
Continuous Internal Evaluation: 0 Marks	Semester End Exam: 0 Marks
Pre requisites: Disaster Risk Assessment, Emergency Response Planning, Community Awareness and Education, Resource Management and Logistics, Coordination with Agencies and Stakeholders	

Course Objectives: -

Students will be able to:

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes: -

CO1	Analyze and differentiate between various types of disasters, including natural and manmade, and their significance in different contexts.
CO2	Assess the economic and ecological repercussions of disasters, including the impact on human and animal life, as well as ecosystem destruction.
CO3	Identify and evaluate disaster-prone areas in India, focusing on specific hazards such as earthquakes, floods, and cyclones, and their associated risks.
CO4	Develop disaster preparedness strategies, including risk evaluation techniques and the use of remote sensing and data from various agencies for effective management.
CO5	Formulate disaster risk assessment and mitigation strategies, emphasizing community participation and emerging trends in disaster management practices.

Syllabus

Unit-1

Introduction, Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Unit-2

Repercussions Of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man- made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Unit-3

Disaster Prone Areas in India Study of Seismic Zones: Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics .

Unit-4

Disaster Preparedness and Management Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

Unit-5

Risk Assessment & Disaster Mitigation

Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival. Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

References:

1.R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies ""New Royal book Company.

2.Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.

3.Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., New Delhi.

Mixed Signal & RF IC Design

Course Title: Mixed Signal & RF IC Design	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PC05
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Analog Circuit Theory, Digital Circuit Design, Semiconductor Device Physics, Electromagnetic Theory, Communication Systems.	

Course Objectives:

- To understand the design of basic cells like Op-Amp, against process and temperature variations meeting the mixed signal specifications.
- To be able to design comparators that can meet the high speed requirements of digital circuitry.
- To be able to design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching.
- To understand the design bottlenecks specific to RF IC design, linearity related issues, and ISI.
- To have a comprehensive idea about different multiple access techniques, wireless standards and various transceiver architectures.

Course Outcomes:

At the end of the course, students will be able to:

CO1	Design basic cells like Op-Amp, against process and temperature variations meeting the mixed signal specifications
CO2	Design comparators that can meet the high speed requirements of digital circuitry.
CO3	Design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching.
CO4	Understand the design bottlenecks specific to RF IC design, linearity related issues and ISI
CO5	Comprehend different multiple access techniques, wireless standards and various transceiver architectures

UNIT -I

Basic Building Blocks, Op-Amp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic- In sensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit

UNIT -II

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity

Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate for Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters.

UNIT -III:

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations of the Second-Order Small-Signal Model, PLL Design Example, Jitter and Phase Noise, Period Jitter , P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators , Oscillators , phase Noise of Oscillators, jitter and Phase Noise in PLLS.

UNIT -IV:

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology. BASICCONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT -V:

Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.

Transceiver Architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

Amplifiers, Mixers And Oscillators: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

Text Books:

1. David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2. R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986

Reference Books:

1. Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008.
2. Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001
3. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits, Cambridge University Press.

Web References:

1. https://ioe.iitm.ac.in/project/rf-analog-and-mixed-signal-integrated-circuits/
2. https://web.iitd.ac.in/~shouri/eel786/

Physical Design Automation

Course Title: Physical Design Automation	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PC06
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Digital Logic Design, VLSI Design Principles, Circuit Theory, Computer-Aided Design Tools, Programming Skills.	

Course Objectives:

- To understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
- To learn the design algorithms to meet the critical design parameters.
- To know the layout optimization techniques and map them to the algorithms
- To understand proto-type EDA tools and know how to test its efficacy

Course Outcomes:

At the end of the course, students will be able to:

CO1	Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology.
CO2	Adapt the design algorithms to meet the critical design parameters.
CO3	Identify layout optimization techniques and map them to the algorithms
CO4	Develop proto-type EDA tool and test its efficacy.

UNIT -I

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNIT -II:

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

UNIT -III:

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbor pointers, corner stitching, multi-layer operations.

UNIT -IV:

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT -V:

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

Text Books:

1. NaveedShervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

Web References:

1. https://archive.nptel.ac.in/courses/106/105/106105161/
2. https://cse.iitkgp.ac.in/~debdeep/pres/Behrampur/pda.pdf
3. https://onlinecourses.nptel.ac.in/noc21_cs12/preview

Design for Testability
(Elective III)

Course Title: Design for Testability (Elective III)	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE03.1
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Clear Requirements, Modular Design, Simplified Interfaces, Comprehensive Documentation, Automated Testing Framework	

Course Objectives:

- Understand the principles and importance of design for testability (DFT) in integrated circuit design.
- Learn various DFT techniques, including scan design, boundary scan, and built-in self-test (BIST).
- Develop skills in implementing DFT strategies to enhance fault detection and diagnosis.
- Analyze the impact of DFT on manufacturing yield and overall product reliability.

Course Outcomes:

At the end of the course, students will be able to:

CO1	Demonstrate advanced knowledge in the basic faults that occur in digital systems, Testing of stuck at faults for digital circuits, Design for testability.
CO2	Analyze testing issues in the field of digital system design critically for conducting research.
CO3	Solve engineering problems by modeling different faults for fault free simulation in digital circuits.
CO4	Apply appropriate research methodologies and techniques to develop new testing strategies for digital and mixed signal circuits and systems.

UNIT -I

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III:

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test- Per Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits -M.L. Bushnell, V. D. Agrawal, Kluwer Academic publishers.

Reference Books:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

Web References:

1. **https://www.cerc.utexas.edu/~jaa/vlsi/lectures/20-2.pdf**
2. **https://archive.nptel.ac.in/courses/117/105/117105137/**
3. **https://vlsitutor.com/nots/design-for-testability/**

IOT and its Applications
(Elective III)

Course Title: IOT and its Applications (Elective III)	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE03.2
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Understanding of Networking Concepts, Familiarity with Programming Languages, Knowledge of Sensor Technologies, Basics of Data Analytics, Awareness of Cloud Computing Platforms	

Course Objectives:

- Understand the foundational concepts of the Internet of Things (IoT) and its architectural components.
- Explore various IoT communication protocols and standards used in device connectivity.
- Analyze real-world applications of IoT across different sectors, such as healthcare, agriculture, and smart cities.
- Develop skills in designing and implementing IoT solutions, including data collection, processing, and visualization.

Course Outcomes:

At the end of this course, students will be able to

CO1	Apply the Knowledge in IOT Technologies and Data management.
CO2	Determine the values chains Perspective of M2M to IOT.
CO3	Implement the state of the Architecture of an IOT.
CO4	Compare IOT Applications in Industrial & real world.
CO5	Demonstrate knowledge and understanding the security and ethical issues of an IOT.

UNIT I:

Fundamentals of IoT- Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT II: IoT Protocols- IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT III: Design And Development- Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT IV: Data Analytics and Supporting Services- Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG

UNIT V: Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.
Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

Text Books:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017

Reference Books:

1. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015
2. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
3. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Ho¨ ller, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Aves and. David Boyle and Elsevier, 2014.
4. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.
5. Recipes to Begin, Expand, and Enhance Your Projects, 2nd Edition, Michael Margolis, Arduino Cookbook and O"Reilly Media, 2011.

Web References:

1. https://www.javatpoint.com/internet-of-things-applications
2. https://onlinecourses.nptel.ac.in/noc22_cs53/preview
3. https://archive.nptel.ac.in/noc/courses/noc19/SEM1/noc19-ee28/

VLSI Signal Processing
(Elective III)

Course Title: VLSI Signal Processing (Elective III)	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE03.3
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Digital Signal Processing, Linear Algebra, Circuit Theory, Microelectronics, Computer Architecture.	

Course Objectives

- Understand the principles of signal processing and its applications in VLSI systems.
- Explore various algorithms and techniques for digital signal processing (DSP) in VLSI design.
- Gain proficiency in designing VLSI architectures for implementing signal processing algorithms.
- Analyze the performance and optimization of signal processing systems in VLSI applications.

Course Outcomes

On successful completion of the module, students will be able to:

CO1	Ability to modify the existing or new DSP architectures suitable for VLSI.
CO2	Understand the concepts of folding and unfolding algorithms and applications.
CO3	Ability to implement fast convolution algorithms.
CO4	Low power design aspects of processors for signal processing and wireless applications.

UNIT -I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems

Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT-V

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.

Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.

Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches.

Text Books:

1. Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

Web References:

1. https://onlinecourses.nptel.ac.in/noc20_ee44/preview
2. https://www.jct.ac.in/engineering/wp-content/uploads/2021/01/35-vlsi.ppt
3. https://www.sciencedirect.com/science/article/abs/pii/S009052670680037X

Network Security and Cryptography
(Elective IV)

Course Title: Network Security and Cryptography (Elective IV)	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE04.1
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Computer Networks, Information Security Fundamentals, Mathematics for Cryptography, Programming Skills, Operating Systems	

Course Objectives

- Understand the fundamental concepts of network security and the role of cryptography in protecting data.
- Explore various encryption algorithms and techniques for secure communication.
- Analyze security protocols and their applications in different network environments.
- Develop skills in assessing and mitigating security threats and vulnerabilities in networks.

Course Outcomes:

At the end of the course, students will be able to:

CO1	Identify and utilize different forms of cryptography techniques.
CO2	Incorporate authentication and security in the network applications.
CO3	Distinguish among different types of threats to the system and handle the same.

UNIT 1:SECURITY

Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Number Theory

Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT 2: PRIVATE-KEY (SYMMETRIC) CRYPTOGRAPHY

Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES),Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Crypt analysis.

UNIT 3:PUBLIC-KEY (ASYMMETRIC) CRYPTOGRAPHY

RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Crypto graphy, Message Authentication Code, hash functions, message digest algorithms:MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT 4:AUTHENTICATION

IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

UNIT 5:SYSTEM SECURITY

Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Counter measures, Firewalls, Firewall Design Principles, Trusted Systems.

Text Books:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private
3. Communication in a Public World", Prentice Hall, 2nd Edition

Reference Books:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey,
3. "Inside Network Perimeter Security", Pearson Education, 2nd Edition
4. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident

Web References:

1. https://www.geeksforgeeks.org/cryptography-and-network-security-principles/
2. https://onlinecourses.nptel.ac.in/noc22_cs90/preview
3. https://archive.nptel.ac.in/courses/106/105/106105162/

Microcontrollers and Programmable Digital Signal Processors
(Elective IV)

Course Title: Microcontrollers and Programmable Digital Signal Processors (Elective IV)	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE04.2
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Digital Electronics, Embedded Systems, C Programming, Circuit Design, Basic Computer Architecture, Digital Signal Processing Fundamentals, C/C++ Programming, Linear Algebra, Signal Analysis Techniques, Hardware Architecture Knowledge.	

Course Objectives

- Understand the architecture and operation of microcontrollers and programmable digital signal processors (DSPs).
- Develop skills in programming microcontrollers and DSPs for various applications using relevant programming languages.
- Explore interfacing techniques for integrating sensors and actuators with microcontrollers and DSPs.
- Analyze performance metrics and optimization techniques for embedded systems using microcontrollers and DSPs.

Course Outcomes:

At the end of this course, students will be able to

CO1	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
CO2	Identify and characterize architecture of Programmable DSP Processors
CO3	Develop small applications by utilizing the ARM processor core and DSP processor based platform.

UNIT 1:

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT 2:

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pend able Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT 3:

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

UNIT 4:

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT 5:

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking

Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkat ramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH , 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.

Reference Books:

1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
3. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com.

Web References:

1. https://www.tutorialspoint.com/microcontrollers-and-digital-signal-processors
2. https://www.mlritm.ac.in/assets/ece/embedded%20system/02_R20%20I%20Yr%20M.Tech(Embedded%20Systems)%20I%20Sem_Syllabus.pdf

LOW POWER VLSI DESIGN
(Elective IV)

Course Title: LOW POWER VLSI DESIGN (Elective IV)	**I Year- II Semester**
Teaching Scheme (L:T:P): 3:0:0	Course Code: 2472PE04.3
Type of Course: Lecture	Credits: 3
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Digital Logic Design, Circuit Theory, Semiconductor Physics, VLSI Fabrication Technology, Computer Architecture	

Course Objectives

- Understand the principles and techniques of low-power VLSI design, including static and dynamic power reduction strategies.
- Explore circuit-level, architectural, and system-level approaches to minimize power consumption in integrated circuits.
- Gain proficiency in using simulation tools to analyze power performance and optimize designs.
- Investigate emerging technologies and design methodologies for achieving energy-efficient VLSI systems.

Course Outcomes:

At the end of the course, students will be able to:

CO1	Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
CO2	Characterize and model power consumption & understand the basic analysis methods.
CO3	Understand leakage sources and reduction techniques.

UNIT-I: Sources of Power Dissipation

Introduction, Short-Circuit Power Dissipation, Switching Power Dissipation, Dynamic Power for a Complex Gate, Reduced Voltage Swing, Switching Activity, Leakage Power Dissipation, p–n Junction Reverse-Biased Current, Band-to-Band Tunneling Current, Sub threshold Leakage Current, Short-Channel Effects.

UNIT 2: Supply Voltage Scaling for Low Power

Device Feature Size Scaling, Constant-Field Scaling, Constant-Voltage Scaling, Architectural-Level Approaches: Parallelism for Low Power, Pipelining for Low Power, Combining Parallelism with Pipelining, Voltage Scaling Using High-Level Transformations: Multilevel Voltage Scaling Challenges in MVS Voltage Scaling Interfaces, Static Timing Analysis Dynamic Voltage and Frequency Scaling.

UNIT-3: Switched Capacitance Minimization

Probabilistic Power Analysis: Random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Bus Encoding: Gray Coding, One-Hot Coding, Bus-Inversion, T0 Coding, Clock Gating, Gated-Clock FSMs FSM State Encoding, FSM Partitioning, Pre computation, Glitching Power Minimization.

UNIT 4: Leakage Power Minimization

Fabrication of Multiple Threshold Voltages, Multiple Channel Doping, Multiple Oxide CMOS, Multiple Channel Length, Multiple Body Bias, VTCMOS Approach, MTCMOS Approach, Power Gating, Clock Gating Versus Power Gating, Power-Gating Issues, Isolation Strategy, State Retention Strategy, Power-Gating Controller, Power Management, Combining DVFS and Power Management.

UNIT 5: Low power clock distribution & Simulation Power Analysis

Low power clock distribution: Power dissipation in clock distribution, single driver versus distributed buffers, zero skew versus tolerable skew, chip and package co design for clock network.

Simulation Power Analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, architecture level analysis, data correlation analysis of DSP systems, Monte Carlo Simulation.

Text Books:

1. Low-Power VLSI Circuits and Systems, Ajit Pal, SPRINGER PUBLISHERS
2. Practical Low Power Digital VLSI Design , Gary Yeap Motorola, Springer Science Business Media, LLC.

Reference Books:

1. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
2. MassoudPedram, Jan M. Rabaey , “Low power design methodologies “, Kluwer Academic Publishers.
3. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

Web References:

1. https://www.maven-silicon.com/blog/what-is-low-power-design-in-vlsi/
2. https://archive.nptel.ac.in/courses/106/105/106105034/
3. https://onlinecourses.nptel.ac.in/noc24_ee80/preview

Mixed Signal IC Design Lab

Course Title: Mixed Signal IC Design Lab	**I Year- II Semester**
Teaching Scheme (L:T:P): 0:0:4	Course Code: 2472PC07
Type of Course: Practical	Credits: 2
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Knowledge of Analog Circuit Design, Understanding of Digital Circuit Design, Proficiency in Semiconductor Device Physics, Familiarity with CAD Tools for IC Design, Basics of Signal Processing.	

Course Objectives:

1. Understand the fundamental concepts of mixed-signal circuit design, including analog and digital components.
2. Gain hands-on experience with simulation and modeling tools for mixed-signal IC design.
3. Learn to analyze and optimize the performance of mixed-signal circuits in various applications.
4. Develop skills in layout design and integration of mixed-signal components in VLSI systems.

Course Outcomes:

CO1	Design and simulate mixed-signal circuits using industry-standard software tools.
CO2	Demonstrate the ability to troubleshoot and test mixed-signal ICs in a laboratory setting.
CO3	Analyze the trade-offs between analog and digital performance in mixed-signal systems.
CO4	Collaborate effectively in teams to design and implement complex mixed-signal projects.

Detailed Syllabus: Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design

i. Two stage cross coupled clamped comparator
ii. Strobed Flip-flop

3) Data converter

Cycle 2:

1) Switched capacitor circuits

i. Parasitic sensitive integrator
ii. Parasitic insensitive integrator

2) Design of PLL
3) Design of VCO
4) Bandgap reference circuit
5) Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

Reading:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986.
3. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

Physical Design Automation Lab

Course Title: Physical Design Automation Lab	**I Year- II Semester**
Teaching Scheme (L:T:P): 0:0:4	Course Code: 2472PC08
Type of Course: Practical	Credits: 2
Continuous Internal Evaluation: 25 Marks	Semester End Exam: 75 Marks
Pre requisites: Digital Logic Design, VLSI Design, Circuit Theory, Electronic Devices, Computer-Aided Design (CAD) Tools.	

Course Objectives:

1. Understand the principles of physical design in VLSI systems, including layout, placement, and routing techniques.
2. Gain proficiency in using industry-standard EDA tools for design automation and optimization.
3. Analyze and apply algorithms for various stages of physical design, focusing on performance, area, and power.
4. Develop skills to evaluate and address design constraints and trade-offs in complex VLSI circuits

Course Outcomes:

CO1	Demonstrate the ability to design and optimize VLSI layouts using automated tools.
CO2	Effectively apply algorithms for placement and routing to enhance circuit performance.
CO3	Critically assess physical design strategies and their impact on overall system functionality.
CO4	Collaborate in teams to solve real-world design challenges, integrating learned techniques and tools.

Detailed syllabus: Cycle 1:

1) Graph algorithms
a) Graph search algorithms
i. Depth first search
ii. Breadth first search
b) Spanning tree algorithm
i. Kruskal‟s algorithm
c) Shortest path algorithm
i. Dijkstra algorithm
ii. Floyd- Warshall algorithm
d) Steiner tree algorithm
2) Computational geometry algorithm
a) Line sweep method
b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms
I) Group migration algorithms
a) Kernighan –Lin algorithm

b) Extensions of Kernighan-Lin algorithm
i) Fiduccias –Mattheyses algorithm
ii) Goldberg and Burstein algorithm
II) Simulated annealing and evolution algorithms
a) Simulated annealing algorithm
b) Simulated evolution algorithm
III) Metric allocation method
4) Floor planning algorithms
i) Constraint based methods
ii) Integer programming based methods
iii) Rectangular dualization based methods
iv) Hierarchical tree based methods
v) Simulated evolution algorithms
vi) Time driven Floorplanning algorithms
5) Routing algorithms
I) Two terminal algorithms
a) Maze routing algorithms
i) Lee‟s algorithm
ii) Soukup‟s algorithm
iii) Hadlock algorithm
b) Line-Probe algorithm
c) Shortest path based algorithm
II) Multi terminal algorithm
a) Stenier tree based algorithm
i) SMST algorithm
ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Reading:

1. Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

MINI PROJECT

Course Title: MINI PROJECT	**I Year- II Semester**
Teaching Scheme (L:T:P): 0:0:4	Course Code: 2472PR01
Type of Course: Practical	Credits: 2
Continuous Internal Evaluation: 100 Marks	Semester End Exam: 0 Marks
Pre requisites:	

Syllabus Contents

The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

Course Outcomes

At the end of this course, students will be able to

CO1	Understand of contemporary / emerging technology for various processes and systems.
CO2	Share knowledge effectively in oral and written form and formulate documents

VALUE EDUCATION

Course Title: VALUE EDUCATION	**I Year- II Semester**
Teaching Scheme (L:T:P): 2:0:0	Course Code: 2472AC02.1
Type of Course: Lecture	Credits: 0
Continuous Internal Evaluation: 0 Marks	Semester End Exam: 0 Marks
Pre requisites: Awareness of Personal Values, Understanding of Ethical Principles, Empathy and Compassion, Critical Thinking Skills, Commitment to Lifelong Learning.	

Course Objectives

Students will be able to

1. Understand value of education and self- development
2. Imbibe good values in students
3. Let the should know about the importance of character

Course outcomes

Students will be able to

CO1	Knowledge of self-development
CO2	Learn the importance of Human values
CO3	Developing the overall personality

Syllabus

Unit-1

Values and self-development

Social values and individual attitudes. Work ethics, Indian vision of humanism, Moral and non-moral valuation. Standards and principles, Value judgements.

Unit-2

Importance of cultivation of values.

Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness, Honesty, Humanity. Power of faith, National Unity, Patriotism, Love for nature ,Discipline.

Unit-3

Personality and Behavior Development

Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labor, Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature. Character and Competence –Holy books vs Blind faith, Self-management and Good health, Science of reincarnation, Equality, Nonviolence ,Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

1 Chakraborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

CONSTITUTION OF INDIA

Course Title: CONSTITUTION OF INDIA	**I Year- II Semester**
Teaching Scheme (L:T:P): 2:0:0	Course Code: 2472AC02.2
Type of Course: Lecture	Credits: 0
Continuous Internal Evaluation: 0 Marks	Semester End Exam: 0 Marks
Pre requisites: Preamble, Fundamental Rights, Directive Principles of State Policy, Fundamental Duties, Amendment Procedure.	

Course Objectives:

Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals‟ constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes:

CO1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
CO2	Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
CO3	Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
CO4	Discuss the passage of the Hindu Code Bill of 1956.

Syllabus

Unit-1

History of Making of the Indian Constitution: History, Drafting Committee, (Composition & Working)

Unit-2

Philosophy of the Indian Constitution, Preamble Salient Features

Contours of Constitutional Rights & Duties:

Fundamental Rights Right to Equality Right to Freedom. Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights. Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties.

Unit-3

Organs of Governance: Parliament Composition, Qualifications and Disqualifications Powers and Functions Executive President Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications Powers and Functions.

Unit-4

Local Administration:

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation. Panchayat raj: Introduction, PRI: Zila Panchayat. Elected officials and their roles, CEO Zila Panchayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy

Unit-5

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

References:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

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Department of ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M.Tech- VLSI Design **Regulation: R24**

I Year I Semester- Course Structure

S.No	Category	Course Code	Course Title	Hours per Week			
				L	T	P	Credits
1	PC	R2457PC01	CMOS Analog IC Design	3	0	0	3
2	PC	R2457PC02	CMOS Digital IC Design	3	0	0	3
3	PE	R2457PE01.1 R2457PE01.2 R2457PE01.3	**Professional Elective-1** 1. VLSI Technology 2. Nanomaterials and Nanotechnology 3. MEMS Technology	3	0	0	3
4	PE	R2457PE02.1 R2457PE02.2 R2457PE02.3	**Professional Elective-2** 1. Device Modeling 2. Nano-electronics 3. Photonics	3	0	0	3
5	PC	R2457PC03	CMOS Analog IC Design Lab	0	0	4	2
6	PC	R2457PC04	CMOS Digital IC Design Lab	0	0	4	2
7	MC	R24MTMC01	Research methodology and IPR	2	0	0	2
8	AC	R24MTAC01.1 R24MTAC01.2	**Audit Course-1** 1. English for Research paper writing 2. Disaster Management	2	0	0	0
			Total	16	0	8	18

Category	Courses	Credits
PC- Professional Core Course	4	10
PE- Professional Elective	2	6
MC-Mandatory Course	1	2
AC- Audit Course	1	0
Total	**8**	**18**

Department of ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M.Tech- VLSI Design **Regulation: R24**

I Year II Semester- Course Structure

S.No	Category	Course Code	Course Title	Hours per Week			
				L	T	P	Credits
1	PC	R2457PC05	Mixed Signal & RF IC Design	3	0	0	3
2	PC	R2457PC06	Physical Design Automation	3	0	0	3
3	PE	R2457PE03.1 R2457PE03.2 R2457PE03.3	**Professional Elective-3** 1. Design For Testability 2. IOT & its Applications 3. VLSI Signal Processing	3	0	0	3
4	PE	R2457PE04.1 R2457PE04.2 R2457PE04.3	**Professional Elective-4** 1. Network Security & Cryptography 2. Microcontrollers & programmable Digital Signal Processors 3. Low Power VLSI Design	3	0	0	3
5	PC	R2457PC07	Mixed Signal IC Design Lab	0	0	4	2
6	PC	R2457PC08	Physical Design Automation Lab	0	0	4	2
7	PR	R2457PR01	Mini Project	0	0	4	2
8	AC	R2457AC02.1 R2457AC02.2	**Audit Course – 2** 1. Constitution of India 2. Value Education	2	0	0	0
			Total	14	0	12	18

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

Category	Courses	Credits
PC- Professional Core Course	4	10
PE- Professional Elective	2	6
PR-Mini Project	1	2
AC- Audit Course	1	0
Total	**8**	**18**

Department of ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M.Tech- VLSI Design **Regulation: R24**

II Year I Semester- Course Structure

S. No.	Category	Course Type/Code	Subject	Teaching Scheme			Credits
				L	T	P	
1	**PE**	R2457PE05.1 R2457PE05.2 R2457PE05.3	a) Scripting Languages for VLSI b) Digital System Design & Verification c) Hardware Software co-design	3	0	0	3
2	**OE**	R2457OE01.1 R2457OE01.2 R2457OE01.3 R2457OE01.4 R2457OE01.5 R2457OE01.6	a) Business Analytics b) Industrial Safety c) Operations Research d) Cost Management of Engineering Projects e) Composite Materials f) Waste to Energy	3	0	0	3
3	**DP**	R2457DP01	Dissertation Phase – I	0	0	20	10
		Total		**6**	**0**	**20**	**16**

Category	Courses	Credits
PE- Professional Elective	**1**	**3**
OE- Open Elective	**1**	**3**
DP- Dissertation Phase-I	**1**	**10**
Total	**3**	**16**

II Year II Semester- Course Structure

S.No.	Category	Course Code	Subject	Teaching Scheme			Credits
				L	T	P	
1	DP	Dissertation	Dissertation Phase – II	--	--	32	16
		Total Credits		--	--	32	**16**

Course Title: SCRIPTING LANGUAGES FOR VLSI	**Course Code:** R2457PE05.1
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in Scripting Languages for VLSI, students should have a solid understanding of digital logic design and VLSI design fundamentals, as these provide the architectural context for automation tasks. Familiarity with basic programming concepts is essential to grasp scripting techniques, and knowledge of hardware description languages (HDLs) like Verilog or VHDL is helpful for understanding automation in synthesis and verification workflows.	

Course Objective

1. To introduce scripting languages and their role in VLSI automation and design flows.
2. To develop proficiency in using PERL for data handling, pattern matching, and scripting.
3. To explore advanced PERL concepts such as modules, objects, and file handling.
4. To enable students to apply TCL/TK for scripting in EDA tools and automation.
5. To impart knowledge of Python as a versatile language for VLSI design and test automation.

Course Outcomes

At the end of this course, students will be able to

Course Outcome (CO)	PO1	PO2	PO3	PO4	PO5	PO11	PSO1	BT LEVEL
CO1: Understand the basics and importance of scripting languages in VLSI workflows.	3	2						L2
CO2: Apply PERL for file handling, data parsing, and automation scripts.	3	3			2			L3
CO3: Develop reusable and modular code using advanced PERL and object-oriented techniques.		3	2		2			L4
CO4: Design automation scripts using TCL/TK and implement event-driven scripting.		3	2	2	3			L5
CO5: Utilize Python for modular scripting and error-handling in VLSI-related applications.	3	2			2	1		L3

SYLLABUS

UNIT-I:

Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scriptingtoday, Characteristics and uses of scripting languages. PERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions,Control structures, Built-in functions, Collections of Data, working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts witharguments. **--CO1,CO2**

UNIT-II:

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objectsand modules in action, tied variables, interfacing to the operating systems, Security issues. **--CO1,CO2,CO3**

UNIT-III:

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL,Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns,Filesand Pipes, Example code. **--CO4**

UNIT-IV:

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages,Namespaces, trapping errors, Event-driven programs, Making applications 'Internet aware','Nuts-and-bolts' internet programming, Security issues, TCL and TK integration. **--CO4**

UNIT-V:

PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in functionsand Methods, Modules in PYTHON, Exception Handling. **--CO5**

Text Books:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications

References:

1. TCL/TK: A Developer's Guide- ClifFlynt, 2003, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pearson Education, 2006.
3. Learning Perl, Randal L. Schwartz, O‟ Reilly publications 6th edition 2011.
4. Linux: The Complete Reference”, Richard Peterson McGraw Hill Publications, 6th Edition,2008.

Course Title: DIGITAL DESIGN AND VERIFICATION	**Course Code:** R2457PE05.2
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in Digital Design and Verification, students should have a solid understanding of basic digital logic design and Boolean algebra, as these are essential for constructing and analyzing digital circuits. Familiarity with combinational and sequential circuits, finite state machines, and hardware description languages (HDLs) such as Verilog or VHDL is important for modeling and simulation.	

Course Objective

1. To review and strengthen foundational concepts in digital systems including FSMs and essential logic blocks.
2. To introduce HDL design methodologies using Verilog and explore IP integration and prototyping techniques.
3. To provide understanding of SystemVerilog for verification, including assertions, OOP concepts, and BIST.
4. To explain current challenges in physical design such as delays, noise, IR drop, and process variations.
5. To study the evolution, architecture, and applications of PLDs, FPGAs, and ASIC design flows.

Course Outcomes

At the end of this course, students will be able to

Course Outcome (CO)	PO1	PO2	PO3	PO4	PO5	PO7	PO8	PO9	PSO1	BT Level
CO1:Understand and analyze digital systems, FSMs, and core building blocks like ALU, FIFO, counters.	3	2			2					L2
CO2:Apply Verilog HDL for modeling combinational/sequential circuits and create testbenches.	3	3	2		3					L3
CO3:Design and verify logic using SystemVerilog features including OOP, assertions, and testbenches.	2	3	3	2	3		1	1		L3
CO4:Identify and analyze physical design challenges like IR drop, noise, wire delay, and process effects.	2	3	2	2	3	2				L4
CO5:Compare and interpret PLD, FPGA architectures, and understand ASIC design flow and programmability.	3	2								L2

SYLLABUS

UNIT I

Revision of basic Digital systems: Combinational Circuits, Sequential Circuits, Logic families.Synchronous FSM and asynchronous design, Meta-stability, Clock distribution and issues, basicbuilding blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth'smultiplier, ALU, Barrel shifter etc. **-CO1**

UNIT II

Verilog/VHDL Comparisons and Guidelines, Verilog: HDL fundamentals, simulation, and testbenchdesign, Examples of Verilog codes for combinational and sequential logic, Verilog AMS. IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP,Netlist, Physical IP, and Use of external hard IP during prototyping, Case studies, and Speedissues. **-CO2**

UNIT III

System Verilog and Verification: Verification guidelines, Data types, procedural statements androutines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization. Testing of logic circuits: Fault models, BIST, JTAG interface Introduction to basic scripting language: Perl, Tcl/Tk. **-CO3**

UNIT IV

Current challenges in physical design: Roots of challenges, Delays: Wire load models GenericPDflow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop,Process effects: Process Antenna Effect &Electro migration. **-CO4**

UNIT V

Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's,Applications, Programming PLD's, FPGA with technology: Anti-fuse, SRAM, EPROM, MUX,FPGA structures, and ASIC Design Flows, Programmable Interconnections, Coarse grainedreconfigurable devices **-CO5**

Text Books:

1. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing &
2. Simulating ASICs & FPGAs Using VHDL or Verilog”, Doone publications, 1998.
3. Samir Palnitkar, “Verilog HDL: A guide to Digital Design and Synthesis”, Prentice Hall,2nd Edition, 2003.

Reference Books:

1. Doug Amos, Austin Lesea, Rene Richter, “FPGA based Prototyping Methodology Manual”, Synopsys Press, 2011.
2. Christophe Bobda, “Introduction to Reconfigurable Computing, Architectures, Algorithmsand Applications”, Springer, 2007.
3. Janick Bergeron, “Writing Testbenches: Functional Verification of HDL Models”, SecondEdition, Springer, 2003.

Course Title: HARDWARE SOFTWARE CO-DESIGN	**Course Code:** R2457PE05.3
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in Hardware Software Co-Design**,** students should have a solid understanding of digital logic design and computer organization, which are essential for comprehending the hardware aspects of embedded systems. A good grasp of microprocessors/microcontrollers**,** C/C++ programming**,** and basic embedded system concepts is crucial for software development and integration.	

Course Objective

1. To understand co-design principles, models, architectures, and methodologies used in hardware-software systems.
2. To learn co-synthesis techniques including partitioning and distributed system synthesis.
3. To explore prototyping and emulation strategies for target embedded architectures.
4. To understand compilation tools, verification techniques, and design specifications in co-design environments.
5. To evaluate system-level specification languages and apply them in multi-language co-simulation contexts.

Course Outcomes

At the end of this course, students will be able to

Course Outcome (CO)	PO1	PO2	PO3	PO4	PO5	PO8	PO9	PO10	BT LEVEL
CO1:Understand co-design principles, languages, and methodologies for integrated hardware-software development.	3	2			2				L2
CO2:Analyze hardware-software partitioning and co-synthesis algorithms for efficient embedded system design.	3	3	2	2	2				L4
CO3:Apply emulation and prototyping techniques for different target architectures in embedded system design.	3	2	2		3				L3
CO4:Evaluate and implement compilation tools and verification strategies in hardware-software co-design workflows.	3	3	3	2	2	1	1	1	L5
CO5:Use and differentiate system-level specification languages and perform multi-language co-simulation.	2	3	2		3				L3,L4

SYLLABUS

UNIT I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis. **-CO1,CO2**

UNIT II

Prototyping and Emulation Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure Target Architectures Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems. **-CO3**

UNIT III

Compilation Techniques and Tools for Embedded Processor Architectures Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment. **-CO4**

UNIT-IV: Design Specification and Verification Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification. **-CO4**

UNIT V

Languages for System-Level Specification and Design-I System-level specification, design representation for system level synthesis, system level specification languages. Languages for System-Level Specification and Design-II Heterogeneous specifications and multi language co-simulation, the cosyma system and Lycos system. **-CO5**

Text Books:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli , Mariagiovanna Sami , 2002, Kluwer Academic Publishers.

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.

Course Title: BUSINESS ANALYTICS	**Course Code: R2457OE01.1**
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in Business Analytics, students should have a solid understanding of statistics, probability, and data interpretation, along with fundamental programming or spreadsheet skills.	

Course Objectives:

1. To introduce the fundamentals, scope, and competitive importance of Business Analytics.
2. To equip students with statistical and regression tools for data-driven decision-making.
3. To explain the organizational and management aspects involved in business analytics projects.
4. To familiarize learners with forecasting, simulation models, and risk analysis techniques.
5. To develop skills in decision analysis, data storytelling, and current trends in analytics.

Course Outcomes:

At the end of the course, students will able to,

Course Outcome	PO1	PO2	PO3	PO4	PO5	PO6	PO8	PO9	PO10	PSO1	BT Level
CO1: Understand the scope, process, and strategic role of business analytics in gaining competitive advantage.	3	2	–	–	–	2	–	–	–	–	L2
CO2: Apply statistical tools and regression techniques for analyzing business data and uncovering trends.	3	3	–	2	2	–	–	–	–	–	L3
CO3: Analyze organizational structures, data management policies, and change management practices in analytics projects.	3	3	2	–	2	2	2	2	2	–	L4
CO4: Use forecasting models, Monte Carlo simulations, and risk analysis techniques for business decision-making.	3	3	3	3	3	–	–	–	–	–	L5
CO5: Evaluate decision problems using decision trees, utility theory, and explore current trends such as data storytelling and embedded analytics.	3	2	3	3	2	–	2	3	2	2	L5

SYLLABUS

UNIT I:

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview. **COs-CO1**

UNIT II:

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology. **COs-CO2**

UNIT III:

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization. **COs-CO3**

UNIT IV:

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte CarleSimulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model. **COs-CO4**

UNIT V:

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

Recent Trends in : Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism. **COs-CO5**

Reference:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FTPress.
2. Business Analytics by James Evans, personsEducation.

Course Title: INDUSTRIAL SAFETY	**Course Code: R2457OE01.2**
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in Business Analytics, students should have a solid understanding of mechanical and electrical systems, engineering materials,industrial processes and tools.	

Course Objectives:

1. Provide a comprehensive understanding of industrial safety, accident prevention, and legal safety frameworks.
2. Impart the knowledge of maintenance engineering principles and strategies.
3. Educate students on wear and corrosion, their impact, and prevention techniques.
4. Develop skills for systematic fault tracing in various equipment and systems.
5. Equip students with methods and schedules for effective periodic and preventive maintenance.

Course Outcomes:

At the end of the course, students will able to,

Course Outcomes (COs)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	BT Level
CO1: Explain industrial accidents, safety measures, and legal requirements (Factories Act 1948).	2	1	–	–	–	3	2	L2
CO2: Describe maintenance engineering principles, types of maintenance, and tools used.	2	2	–	–	2	–	–	L2
CO3: Analyze causes of wear and corrosion and select suitable lubrication techniques.	2	3	–	2	2	–	2	L3
CO4: Apply fault tracing techniques and draw decision trees for common equipment faults.	2	3	–	3	3	–	–	L3
CO5: Develop preventive maintenance schedules and programs for electrical and mechanical equipment.	3	3	2	2	2	–	3	L4

SYLLABUS

UNIT I :

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods. **COs-CO1**

UNIT II:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy,

Service life of equipment. **COs-CO2**

UNIT III:

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods. **COs-CO3**

UNIT IV:

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment‟s like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine,v. Boiler,vi .Electrical motors, Types of faults in machine tools and their general causes. **COs-CO4**

UNIT V:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii.Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept andimportance. **COs-CO5**

Reference:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da InformationServices.
2. Maintenance Engineering, H. P. Garg, S. Chand andCompany.
3. Pump-hydraulic Compressors, Audels, McgrewHillPublication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman &HallLondon

Course Title: OPERATIONS RESEARCH	**Course Code: R2457OE01.3**
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in Operations Research, students should have a solid understanding of mathematics (algebra, calculus),Matrix operations, linear equations, probability, statistics, Logical reasoning and analytical skills.	

Course Objectives:

1. Introduce mathematical modeling techniques used in decision making.
2. Teach various optimization techniques including linear, nonlinear, and dynamic programming.
3. Equip students with skills to solve real-life problems using simplex, duality, sensitivity analysis, and simulation.
4. Explain scheduling, sequencing, and inventory models.
5. Enable students to apply game theory, network flow, and probabilistic models for effective planning and control.

Course Outcomes:

At the end of the course, students will able to,

Course Outcomes (COs)	PO1	PO2	PO3	PO4	PO5	PSO1	BT Level
CO1: Formulate and solve linear programming problems using graphical and simplex methods.	3	3	–	2	2		L3
CO2: Apply duality, revised simplex, and sensitivity analysis to evaluate impacts of parameter changes.	3	3	–	2	2		L4
CO3: Solve nonlinear programming and network models like minimum cost and maximum flow problems.	3	3	–	3	2		L4
CO4: Apply scheduling, sequencing, and inventory models (deterministic and probabilistic) to optimize resource usage.	2	3	–	3	3		L3
CO5: Apply game theory, dynamic programming, and simulation techniques to solve competitive and stochastic problems.	3	3	–	3	3		L4

SYLLABUS

UNIT I :
Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models **COs-CO1**

UNIT II
Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming. **COs-CO2**

UNIT III:
Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT. **COs-CO3**

UNIT IV:
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming. **COs-CO4**

UNIT V:
Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation **COs-CO5**

REFERENCES:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

Course Title: COST MANAGEMENT OF ENGINEERING PROJECTS	**Course Code: R2457OE01.4**
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in cost management of engineering projects , students should have a solid understanding of accounting and cost principles, Familiarity with project lifecycle concepts, decision-making tools and mathematical fundamentals	

Course Objectives:

1. To introduce strategic cost management concepts and tools used in decision-making.
2. To develop the ability to plan, execute, and control technical and non-technical aspects of projects.
3. To apply cost behavior, variance analysis, and planning techniques in managerial decisions.
4. To integrate modern tools like ERP, TQM, and benchmarking into cost management systems.
5. To utilize quantitative and optimization techniques in budgeting, pricing, and project evaluation.

Course Outcomes:

At the end of the course, students will able to,

Course Outcomes (COs)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO10	PSO1	BT Level
CO1: Explain cost concepts, relevant costing, and use of data in decision-making.	3	3	–	2	2	–	–	–	–	–	L2
CO2: Describe stages of project planning and execution with documentation and legal clearances.	3	3	–	2	2	2	–	–	–	–	L2
CO3: Apply cost control, scheduling tools, and teamwork concepts in project execution and commissioning.	2	3	3	3	3	3	2	–	2	–	L3
CO4: Analyze cost behaviors, profit planning, pricing strategies, and variance analysis for business decisions.	3	3	2	3	2	–	–	–	–	–	L4
CO5: Evaluate advanced cost management methods like ABC, TQM, Benchmarking, and apply quantitative models for cost optimization.	3	3	3	3	3	3	–	2	–	–	L5

SYLLABUS

UNIT-I

Introduction and Overview of the Strategic Cost Management Process, Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System;

Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making. **COs-CO1**

UNIT-II

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non-technical activities.Detailed Engineering activities. Pre project execution main clearances and documents.

COs-CO2

UNIT-III

Project team: Role of each member. Importance Project site: Data required with significance. Project contracts.Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process. **COs-CO3**

UNIT-IV

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector.Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning. **COs-CO4**

UNIT-V

Total Quality Management and Theory of constraints.Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value- Chain Analysis.Budgetary Control; Flexible Budgets;Performance budgets; Zero-based budgets.Measurement of Divisional profitability pricing decisions including transfer pricing. Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory. **COs-CO5**

REFERENCES:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

Course Title: COMPOSITE MATERIALS	**Course Code: R2457OE01.5**
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in composite materials, students should have a solid understanding of materials science and mechanical properties of engineering materials and Familiarity with conventional manufacturing processes.	

Course Objectives:

1. To understand the fundamentals, types, and benefits of composite materials.
2. To learn the behavior and application of various reinforcements and matrices.
3. To explore manufacturing techniques for metal, ceramic, carbon, and polymer matrix composites.
4. To analyze the mechanical behavior and performance of composite structures.
5. To apply strength and failure criteria for design of composite laminates.

Course Outcomes:

At the end of the course, students will able to,

Course Outcomes (COs)	PO1	PO2	PO3	PO4	PO5	PO11	BT Level
CO1: Explain the classification, characteristics, and advantages of composites and reinforcement effects on performance.	3	3	–	2	2	–	L2
CO2: Describe the types, properties, and preparation techniques of various reinforcements and evaluate their mechanical behavior.	3	3	–	3	–	–	L4
CO3: Explain the manufacturing methods for metal, ceramic, and carbon–carbon composites and their applications.	3	3	2	2	3	–	L2
CO4: Illustrate and compare manufacturing processes of polymer matrix composites and evaluate their suitability in various applications.	3	3	2	3	2	–	L4
CO5: Apply strength and failure criteria for composite laminates and analyze stress-strain behavior under loading.	3	3	3	3	3	–	L5

SYLLABUS

UNIT–I:

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix.Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance. **COs-CO1**

UNIT – II:

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements.

Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions. **COs-CO2**

UNIT – III:

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostaticpressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications. **COs-CO3**

UNIT–IV:

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications. **COs-CO4**

UNIT – V:

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations. **COs-CO5**

TEXT BOOKS:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition,2007.

REFERENCES:

1. Hand Book of CompositeMaterials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L.Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

Course Title: WASTE TO ENERGY	**Course Code: R2457OE01.6**
Teaching Scheme (L:T:P): 3:0:0	**Credits:** 03
Type of Course: Lecture	
Continuous Internal Evaluation: 30 Marks	**Semester End Exam:** 70 Marks
Pre requisites: To succeed in waste to energy, students should have a solid understanding of thermodynamics, heat transfer, and environmental science,Awareness of renewable energy systems and energy conversion technologies.	

Course Objectives:

1. To classify different types of waste and identify suitable conversion technologies.
2. To study biomass conversion methods like pyrolysis, gasification, and combustion.
3. To understand the construction and working of various biomass and waste-to-energy systems.
4. To analyze energy yield, performance, and applications of waste-to-energy technologies.
5. To explore the status, design, and applications of biogas and biofuel systems in India.

Course Outcomes:

At the end of the course, students will able to,

Course Outcomes (COs)	PO1	PO2	PO3	PO4	PO5	PSO1	BT Level
CO1: Classify waste resources and describe different energy conversion devices like incinerators, gasifiers, and digestors.	3	3	–	2	2	–	L2
CO2: Explain types of pyrolysis, methods for charcoal production, and applications of pyrolytic oils and gases.	3	2	–	2	2	–	L2
CO3: Analyze biomass gasifiers, their design and operation, and assess performance in thermal and electrical applications.	3	3	3	3	3	–	L4
CO4: Illustrate and compare combustion technologies like biomass stoves, chullahs, and fluidized bed combustors.	3	3	2	3	2	–	L4
CO5: Evaluate biogas systems, conversion technologies, and biofuel production processes with reference to India's biomass energy programme.	3	3	3	3	3	–	L5

UNIT-I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors. **COs-CO1**

UNIT-II:

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications. **COs-CO2**

UNIT-III:

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation. **COs-CO3**

UNIT-IV:

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors. **COs-CO4**

UNIT-V:

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India. **COs-CO5**

REFERENCES:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

Course Title: DISSERTATION PHASE – I	**Course Code: R2457DP01**
Teaching Scheme (L:T:P): 0:0: 20	**Credits:** 10
Type of Course: Practicals	

The student should identify a dissertation/project topic relevant to:

- Social needs of society
- Value addition to existing facilities in the institute
- Industry requirements
- National development priorities
- Research and development in the relevant domain

The student is expected to complete the following during Phase–I:

- Literature Survey and Problem Definition
- Motivation and Objectives of the Study
- Preliminary Design / Feasibility Study / Modular Approaches
- Initial Implementation and Proof of Concept (if applicable)
- Regular documentation and presentation of progress

Guidelines for Dissertation Phase – I in M. Tech (VLSID):

- As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
- The dissertation may be carried out preferably in-house i.e. department‟s laboratories and centers OR in industry allotted through department‟s T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.

- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q &A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.

Dr. E. Govinda, HOD

BoS Chairman, Dept of ECE

II YEAR-IISEMESTER

Course Title: DISSERTATION PHASE – II	**Course Code: R2457DP02**
Teaching Scheme (L:T:P): 0:0: 32	**Credits:** 16
Type of Course: Practicals	

The dissertation work from Phase–I is extended into full implementation and testing.

Students are expected to:

- Finalize design and complete development/testing of the proposed system
- Analyze, interpret, and validate results
- Focus on innovation, relevance, and practical applicability
- Prepare and submit a comprehensive dissertation report

The dissertation may involve:

- Experimental verification or proof of concept
- Design, fabrication, and testing of electronic/communication systems
- Software and/or hardware prototypes.

Guidelines for Dissertation Phase – II in M. Tech (VLSID):

- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, a record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q &A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work

Dr. E. Govinda, HOD
BoS Chairman, Dept of ECE