JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE & SYLLABUS M.Tech ECE
VLSI, VLSI Design, VLSI System Design,
VLSI Micro-Electronic Programme

(Applicable for batches admitted from 2019-2020)

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I Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	CMOS Analog IC Design			3	0	0	3
2	PC	CMOS Digital IC design			3	0	0	3
3	PE	1. VLSI Technology 2. Nanomaterials and Nanotechnology 3. MEMS Technology			3	0	0	3
4	PE	1. Device Modeling 2.Nano-electronics 3.Photonics			3	0	0	3
5		Research methodology and IPR			2	0	0	2
6	Lab 1	CMOS Analog IC Design Lab			0	0	4	2
7	Lab 2	CMOS Digital IC Design Lab			0	0	4	2
8	Aud 1	Audit course-1			2	0	0	0
				Total				18

II Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	Mixed Signal & RF IC Design			3	0	0	3
2	PC	Physical Design Automation			3	0	0	3
3	PE	1. Design For Testability 2. IOT & its Applications 3. VLSI Signal Processing			3	0	0	3
4	PE	1.Network Security & Cryptography 2.Microcontrollers & programmable Digital Signal Processors 3. Low Power VLSI Design			3	0	0	3
5	Lab 1	Mixed Signal IC Design Lab			0	0	4	2
6	Lab 2	Physical Design Automation Lab			0	0	4	2
7	MP	Mini Project			0	0	4	2
8	Aud 2	Audit Course – 2			2	0	0	0
				Total				18

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

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III Semester*

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PE	1.Scripting Languages for VLSI 2. Digital System Design & Verification 3.Hardware Software co-design			3	0	0	3
2	OE	1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy			3	0	0	3
3	Dissertation	Dissertation Phase -I /Industrial Project **(to be continued and evaluated next semester)**			0	0	20	10#
				Total				16

#Evaluated and Displayed in IV Semester Marks list.

*Students going for Industrial Project/Thesis will complete these courses through MOOCs

IV Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	Dissertation	Project/ Dissertation Phase-II **(continued from III semester)**			0	0	32	16
				Total				16

Audit Course 1& 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

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I Year I Semester	L	P	C
	0	4	2

CMOS Analog IC Design Lab

- The students are required to design and implement any TEN Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software.
- The students are required to implement LAYOUTS of any SIX Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software. and Compare the results with Pre-Layout Simulation.

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:
Software:
Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator
Hardware:
Personal Computer with necessary peripherals, configuration and operating System.

Course Outcomes:

1. Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools
2. Grasp the significance of various cmos analog circuits in full-custom IC Design flow
3. Have the ability to explain the Physical Verification in Layout Design
4. Fully Appreciate the design and analyze of analog and mixed signal simulation
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

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	L	P	C
I Year I Semester	**0**	**4**	**2**

CMOS Digital IC design Lab

- The students are required to design and implement the Circuit and Layout of any TEN Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software.

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

Course Outcomes:

1. Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools
2. Grasp the significance of various design logic Circuits in full-custom IC Design.
3. Have the ability to explain the Physical Verification in Layout Extraction
4. Fully Appreciate the design and analyze of CMOS Digital Circuits
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

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I Year II Semester

L	P	C
0	4	2

Mixed Signal IC Design Lab

Detailed Syllabus:
Cycle 1:
1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
i. Two stage cross coupled clamped comparator
ii. Strobed Flip-flop
3) Data converter

Cycle 2:
1) Switched capacitor circuits
i. Parasitic sensitive integrator
ii. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Bandgap reference circuit
5) Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

Reading:
1) David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2) R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986.
3) Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4) Alan Hastlings, The art of Analog Layout, Wiley, 2005.

I Year II Semester

L	P	C
0	4	2

Physical Design Automation Lab

Detailed syllabus:
Cycle 1:

1) Graph algorithms
a) Graph search algorithms
i. Depth first search
ii. Breadth first search
b) Spanning tree algorithm
i. Kruskal's algorithm
c) Shortest path algorithm
i. Dijkstra algorithm
ii. Floyd- Warshall algorithm
d) Steiner tree algorithm

2) Computational geometry algorithm
a) Line sweep method
b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms
I) Group migration algorithms
a) Kernighan –Lin algorithm
b) Extensions of Kernighan-Lin algorithm
i) Fiduccias –Mattheyses algorithm
ii) Goldberg and Burstein algorithm
II) Simulated annealing and evolution algorithms
a) Simulated annealing algorithm
b) Simulated evolution algorithm
III) Metric allocation method

4) Floor planning algorithms
i) Constraint based methods
ii) Integer programming based methods
iii) Rectangular dualization based methods
iv) Hierarchical tree based methods
v) Simulated evolution algorithms
vi) Time driven Floorplanning algorithms

5) Routing algorithms

I) Two terminal algorithms
a) Maze routing algorithms
i)Lee's algorithm
ii) Soukup's algorithm
iii) Hadlock algorithm
b) Line-Probe algorithm
c) Shortest path based algorithm
II) Multi terminal algorithm
a) Stenier tree based algorithm
i) SMST algorithm
ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Reading:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

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I Year II Semester

L	P	C
0	4	2

MINI PROJECT

Syllabus Contents

The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

Course Outcomes

At the end of this course, students will be able to

1. Understand of contemporary / emerging technology for various processes and systems.
2. Share knowledge effectively in oral and written form and formulate documents