AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, Permanently Affiliated to JNT University Kakinada, Accredited by NAAC and Recognized under 2(f) &12 (b) by UGC, New Delhi)
Tamaram, Makavarapalem, Narsipatnam (RD),
Visakhapatnam-531113

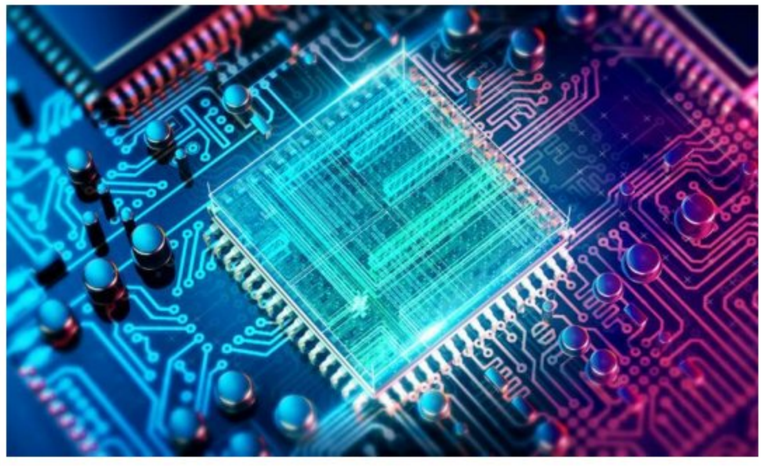
Certificate Course

on

Designing And Verification Of Digital System Using Verilog And Machine Learning

From 15th Feb 2021 to 20th Feb2021

link: https:// meet.google.com/tny-fwdd-fau



ORGANIZED BY

DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING
AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY,
MAKAVARAPALEM (V), VISAKHAPATNAM-531113

AVANTHI EDUCATIONAL SOCIETY

Avanthi Educational Society under the Leadership of Sri M.Srinivasa Rao garu as chairman was started in the Year 1991. Within a short span of its establishment, the group has made a remarkable stride in the field of education offering various courses at Under Graduate, Post Graduate, Pharmacy & Engineering levels. This milestone is achieved as the institution carved itself to impart quality and career oriented education, countering the challenges of the modern world through planning, dedication, determination, prompt execution and with the innovative ideas of our advisory board.

Today, Avanthi Educational Society is proud to have a strength of over 16000 students with 15 institutions under its ambit. It is the path of glory towards the success during the last 19 years. The institution has been adjudged many times as the second best educational institutions in the twin cities and 16th best in all over India through the impartial survey made by the renowned magazine "India Today".

AVANTHI INSTITUTE OF ENGINEERING & TECHNOLOGY

AIET started in the year 1999 and offers various courses at Engineering and PG level. The college is providing with rooms, computer centre, laboratories and seminar hall with audio-visual equipments. Industry Institute interaction is conducted regularly to emphasize on the latest trends in the present market.

It is very near to Narsipatnam. Frequent bus facilities are available both from and to Visakhapatnam and Narsipatnam. Very safe and secure hostel facility is available for Girl students. These are the additional facilities besides excellent academic atmosphere in the college campus.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

The ECE Department was established in the year 1999 with an intake of 60 students and this was increased to 120 students in the 2007 and increased to 180 students in the 2012. The department has an eminent faculty and well supported infrastructure and laboratories. The faculty keeps abreast with the latest advances in technology and ensures that hardware equipment and related software are upgraded to ensure its students are able to keep pace with current trends in technology and the industry.

The department also offers a Post – Graduate courses in DECS and VLSI Design. The students are encouraged to participate in workshops, industrial internship, industrial visits and seminars; along with the projects assigned during the course, these activities enable them to broaden their outlook and build in professionalism that makes their transition from college to industry smoother after graduation.

ABOUT COURSE

Design verification (DV) of integrated circuits typically involves generating stimulus of input signals and then evaluating the resulting output signals against expected values. This allows design simulations to be conducted to determine whether the design is operating correctly. Simulation failures indicate that one or more bugs are present in the design

TOPICS TO BE COVERED

- **Day-1:**Introduction to Verilog HDL
- **Day-2:**Gate Level Modelling
- **Day-3:**Modelling at dataflow level
- **Day-4:**Behavioral Modelling
- **Day-5:**Switch Level Modelling
- **Day-6:**System tasks, Functions and Compiler Directives

For Registration please contact Mr.T.Patala Naidu, Assistant Professor, ECE

CHIEF PATRON	PATRON	CHAIRMAN
Smt.M.Gnaneswari President, Avanthi Educational Society	Dr. C P V N J Mohan Rao Principal, Avanthi Institute Of Engineering And Technology	Sri. E. Govinda Head of the Department Electronics and Communication Engineering

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, Permanently Affiliated to JNT University Kakinada,
ACCREDITED BY NAAC and Recognized under 2(f) &12 (b) by UGC, New Delhi)
Tamaram, Makavarapalem, Narsipatnam (RD), Visakhapatnam-531113

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CIRCULAR

Date: 12/02/2021.

This is informed to all the III B.Tech ECE students that our department is planning to conduct one week course on "**Designing And Verification Of Digital system using Verilog and Machine Learning**" scheduled from 15-02-2021 to 20-02-2021. It is directed to all the students of III ECE to utilize this opportunity to enhance your technical skills. For more details about registration process and participation contact Course Coordinator Mr.T.Patala Naidu, Assistant Professor. ECE.

Resource Person Details:

1. Dr. M.Rajan Babu.
   Professor.
   Department of ECE.
   Lendi Institute of Engineering and Technology.
   Vizianagaram.

2. Dr.J.Sudhakar.
   Professor.
   Department of ECE.
   Vignan's Institute of Engineering for Women.
   Visakhapatnam.

F. Govinda

Head of the Department.

ECE.

HEAD OF THE DEPARTMENT
DEPARTMENT OF ECE
Avanthi Institute of Engg.&Tech.
Makavarapalem, Visakhapatnam Dist-531 113

Copy to: Principal, AIET

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, Permanently Affiliated to JNT University Kakinada,
ACCREDITED BY NAAC and Recognized under 2(f) &12 (b) by UGC, New Delhi)
Tamaram, Makavarapalem, Narsipatnam (RD), Visakhapatnam-531113

Designing and Verification of Digital system using Verilog and Machine Learning

From15th Feb 2021 to 20th Feb 2021

SYLLABUS

- **Day-1:** Introduction to Verilog HDL
- **Day-2:** Gate Level Modeling
- **Day-3:** Modeling at Dataflow Level
- **Day-4:** Behavioral Modeling
- **Day-5:** Switch Level Modeling
- **Day-6:** System Tasks, Functions and Compiler Directives

E.Govinda CHAIRMAN & Head of the Department Electronics and communication Engineering	T.Pattala Naidu Asst. Professor Coordinator

HEAD OF THE DEPARTMENT
DEPARTMENT OF ECE
Avanthi Institute of Engg.&Tech.
Makavarapalem, Visakhapatnam Dist-531 113.

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, Permanently Affiliated to JNT University Kakinada,
ACCREDITED BY NAAC and Recognized under 2(f) &12 (b) by UGC, New Delhi)
Tamaram, Makavarapalem, Narsipatnam (RD), Visakhapatnam-531113

Designing and Verification of Digital system using Verilog and Machine Learning

From 15th Feb 2021 to 20th Feb 2021

Schedule

Day-1 (15/02/2021)

09:00 to 10:00	Inaugural Session
10:00 to 12:00	Introduction to Verilog HDL
12:00 to 01:00	Lunch Break
01:00 to 04:00	Integrated circuits,programmable logic devices

Day-2 (16/02/2021)

09:00 to 12:00	Gate Level Modeling
12:00 to 01:00	Lunch Break
01:00 to 04:00	Explanation of gate level modelling examples

Day-3(17/02/2021)

09:00 to 12:00	Modeling at Dataflow Level
12:00 to 01:00	Lunch Break
01:00 to 04:00	Data flow modelling techniques

Day-4(18/02/2021)

09:00 to 12:00	Behavioral Modeling
12:00 to 01:00	Lunch Break
01:00 to 04:00	Procedural statements,simulation controlling

Day-5(19/02/2021)

09:00 to 12:00	Switch Level Modeling
12:00 to 01:00	Lunch Break
01:00 to 04:00	Explanation of mos switches

Day-6(20/02/2021)

09:00 to 12:00	System Tasks, Functions and Compiler Directives
12:00 to 01:00	Lunch Break
01:00 to 04:00	Terminating simulation and conclusion

E. Govinda
CHAIRMAN
&
Head of the Department
Electronics and Communication Engineering

T.Pattala Naidu
Asst. Professor

Coordinator

HEAD OF THE DEPARTMENT
DEPARTMENT OF ECE
Avanthi Institute of Engg.&Tech.
Makavarapalem, Visakhapatnam Dist-5 3..

AVANTHIINSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, Permanently Affiliated to JNT University Kakinada,
ACCREDITED BY NAAC and Recognized under 2(f) &12 (b) by UGC, New Delhi)
Tamaram, Makavarapalem, Narsipatnam (RD), Visakhapatnam-531113

Designing and Verification of Digital system using Verilog and Machine Learning
from 15th February 2021 to 20th February 2021
III BTECH ECE- I STUDENTS ATTENDANCE LIST

S.NO	Regd No	Name of the Student	15/02	16/02	17/02	18/02	19/02	20/02
1	18811A0401	ARIPAKA MANOHAR	✓	✓	✓	✓	✓	✓
2	18811A0402	ASODA SUMITH GOLDI YUVRAJ	✓	✓	✓	✓	✓	✓
3	18811A0403	BATTINI DIVYASREE	✓	✓	✓	✓	✓	✓
4	18811A0404	BEJAWADA TEJASWI	✓	✓	✓	✓	✓	✓
5	18811A0405	CHALUMURI MAHESH	✓	✓	✓	✓	✓	✓
6	18811A0406	CHINTAKAYALA TULASI	✓	✓	✓	✓	✓	✓
7	18811A0407	CHODISETTI DIVAKAR MANIKANTA NOOKESH	✓	✓	✓	✓	✓	✓
8	18811A0408	CHUKKA REVATHI	✓	✓	✓	✓	✓	✓
9	18811A0409	GANTA JAYA VARDHINI	✓	✓	✓	✓	✓	✓
10	18811A0410	GANTA ROHIT CHOWD ARY	✓	✓	✓	✓	✓	✓
11	18811A0411	GILAKAMSETTI LAVANYA	✓	✓	✓	✓	✓	✓
12	18811A0412	GORLI POOJITHA	✓	✓	✓	✓	✓	✓
13	18811A0413	GORLI TRIVENI	✓	✓	✓	✓	✓	✓
14	18811A0414	GRANDHI LOKESHWAR RAO	✓	✓	✓	✓	✓	✓
15	18811A0415	KARANAM MANIKANTA	✓	✓	✓	✓	✓	✓
16	18811A0416	KOSURI INDIRA	✓	✓	✓	✓	✓	✓
17	18811A0417	MAKIREDDI NIHARIKA	✓	✓	✓	✓	✓	✓
18	18811A0418	NAMBARU MADHUKANTH	✓	✓	✓	✓	✓	✓
19	18811A0419	NANEPALLI BHAGAVAN	✓	✓	✓	✓	✓	✓
20	18811A0420	NEERUKATTU MANOJ	✓	✓	✓	✓	✓	✓
21	18811A0421	PAMPANA SAI SRAVANI	✓	✓	✓	✓	✗	✓
22	18811A0422	PAMPANA SYAMALA	✓	✓	✓	✓	✓	✓
23	18811A0423	PEDIREDLA BHAVANI	✓	✓	✓	✓	✓	✓
24	18811A0424	PERUSOMULA CHANDRA KIRAN	✓	✓	✓	✓	✓	✓
25	18811A0425	POLUPARTI PRAVALLIKA DEVI	✓	✓	✓	✓	✓	✓
26	18811A0426	RAJANA MOUNICA	✓	✓	✓	✓	✓	✗
27	18811A0427	RONGALA SUGUNA	✓	✓	✓	✓	✓	✓
28	18811A0428	RUTTALA PRASAD	✓	✓	✓	✓	✓	✓
29	18811A0429	SAPPA DURGA PRASAD	✓	✓	✓	✓	✓	✓
30	18811A0430	SAYAM SAI SRIRAM	✓	✓	✓	✓	✓	✓
31	18811A0431	SURLA SUNITHA	✓	✓	✓	✓	✓	✓
32	18811A0432	THATTA VENNELA SRI SAI	✓	✓	✓	✓	✓	✓
33	18811A0433	VANTU SATYA SRAVANI	✓	✓	✓	✓	✓	✓
34	18811A0434	VEMULAPUDI YERRANNA	✓	✓	✓	✓	✓	✓

35	18811A0435	YELURI VENKATA SHANMUKHA SATYA NIKHIL	✓	✓	✓	✓	✓	✓
36	18811A0436	YERRA ANUSHA	✓	✓	✓	✓	✓	✓
37	18811A0437	SAKA SHEEBHA ANNAVAJRAM	✓	✓	✓	✓	✓	✓
38	18811A0438	DONDA ANUSHA	✓	✓	✓	✓	✓	✓
39	19815A0401	BODDU PRASANNA GOWRI	✓	✓	✓	✓	✓	✓
40	19815A0402	BONDA BALA BHASKAR	✓	✓	✓	✓	✓	✓
41	19815A0403	CHANDANADA DURGA RAO	✓	✓	✓	✓	✓	✓
42	19815A0404	CHINTAMREDDI SATYA	✓	✓	✓	✓	✓	✓
43	19815A0405	CHITIKELA SAI BALAJI	✓	✓	✓	✓	✓	✓
44	19815A0406	DEVAVARAPU JAYASREE	✓	✓	✓	✓	✓	✓
45	19815A0407	GADE SAI KUMAR	✓	✓	✓	✓	✓	✓
46	19815A0408	GANDEPALLI AJAY	✓	✓	✓	✓	✓	✓
47	19815A0409	GATEREDDI HEMALATHA	✓	✓	✓	✓	✓	✓
48	19815A0410	GOLLAVILLI DEVI	✓	✓	✓	✓	✓	✓
49	19815A0411	GUNDUMALLA SATYA HEMALATHA	✓	✓	✓	✓	✓	✓
50	19815A0412	KARRI RAMU	✓	✓	✓	✓	✓	✓
51	19815A0413	KOLAGANI TIRUMALA	✓	✓	✓	✓	✓	✓
52	19815A0414	KORUPROLU SRINIVASARAO	✓	✓	✓	✓	✓	✓
53	19815A0415	MADDU GRISHMA GAYATHRI	✓	✓	✓	✓	✓	✓
54	19815A0416	MONGAM MAMATHA LAKSHMI	✓	✓	✓	✓	✓	✓
55	19815A0417	NUNNA KARUNYA	✓	✓	✓	✓	✓	✓
56	19815A0418	PEDISETTI SREE SAI SWAPNA	✓	✓	✓	✓	✓	✓
57	19815A0419	POLUMURI AJAY	✓	✓	✓	✓	✓	✓
58	19815A0420	RAMOJU SAI SHANKAR	✓	✓	✓	✓	✓	✓
59	19815A0421	RONGALA CHANDRA LEKHA	✓	✓	✓	✓	✓	✓
60	19815A0422	RONGALA UMA	✓	✓	✓	✓	✓	✓
61	19815A0423	TASUBILLI MOUNIKA	✓	✓	✓	✓	✓	✓

T.P. Reddy
Coordinator

HOD

HEAD OF THE DEPARTMENT
DEPARTMENT OF ECE
Avanthi Institute of Engg.&Tech.,
Makavarapalem, Visakhapatnam Dist-53- 113

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, Permanently Affiliated to JNT University Kakinada,
ACCREDITED BY NAAC and Recognized under 2(f) &12 (b) by UGC, New Delhi)

Tamaram, Makavarapalem, Narsipatnam (RD), Visakhapatnam-531113

Department ofElectronics and Communication Engineering

Dt:24/02/2021

BRIEF REPORT

Avanthi Institute of Engineering and Technology had organized a certificate course on "Designing and Verification of Digital System Using Verilog and Machine Learning" From 15th Feb 2021to 20th Feb 2021 in the Department of Electronics and Communication Engineering.

We had Dr.M.Rajan Babu, Professor,Department of Electronics and Communication Engineering, Lendi Institute of Engineering and Technology, Jonnada, Vizianagaram, shared his knowledge among students ,the information related to hardware description language to help with verification before fabrication so different experiments were done using verilog program.

Dr.J.Sudhakar, Professor, Department of Electronics and Communication Engineering, Vignan's Institute of Engineering for women's, visakhapatnam introduced the concept of modelling techniques such as gate level, behavioral level, data flow level modelling . He also got exposure to the design flow and synthesizing his own HDL codes in to the various development kits from xilinx.

T.P Naidu
Coordinator

Head of the Department

HEAD OF THE DEPARTMENT
DEPARTMENT OF ECE
Avanthi Institute of Engg.&Tech.
Makavarapalem, Visakhapatnam Dist-531 113.

AVANTHI

INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, Permanently Affiliated to JNT University Kakinada,ACCREDITED BY NAAC and Recognized under 2(f) &12 (b) by UGC, New Delhi)

Tamaram, Makavarapalem, Narsipatnam (RD), Visakhapatnam-53111

Certificate of Participation

This is to certify that Mr./Ms._____of _____has participated in the Certificate Course entitled on *Designing and Verification of Digital system using Verilog and Machine Learning* conducted from 15-02-2021 to 20-02-2021 was organized by the Department of ELECTRONICS AND COMMUNICATION ENGINEERING at Avanthi Institute of Engineering and Technology.

Coordinator **HOD** **Principal**