COMPARISON OF FIVE LEVEL, SEVEN LEVEL & NINE LEVEL CASCADED H-BRIDGE MULTI-LEVEL INVERTER

A project report submitted in partial fulfillment of the requirements
For the award of the degree of

BACHELOR OF TECHNOLOGY
IN
ELECTRICAL & ELECTRONICS ENGINEERING

Submitted by

ADAPA SRINIVAS
(18815A0201)

R PRAKASH RAO
(17811A0214)

DHARA KALYAN
(18815A0212)

PANDURI VENKATA SAI KUMAR
(18815A0223)

Under the Esteemed Guidance of

Mr. U ANJAIAH

Assistant Professor

DEPARTMENT OF
ELECTRICAL AND ELECTRONICS ENGINEERING

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Permanently Affiliated to Jawaharlal Nehru Technological University, Kakinada, AP)
(An NAAC Accredited Institution)
Tamaram, Narsipatnam, Visakhapatnam-531113

2020-2021

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Permanently Affiliated to Jawaharlal Nehru Technological University, Kakinada, AP)

(An NAAC Accredited Institution)

Tamaram,Narsipatnam,Visakhapatnam-531113

DEPARTMENT OF
ELECTRICAL AND ELECTRONICS ENGINEERING

CERTIFICATE

This is certify that the project report entitled **"COMPARISON OF FIVE LEVEL, SEVEN LEVEL & NINE LEVEL CASCADED H-BRIDGE MULTI-LEVEL INVERTER"** is a bonafide work submitted by **ADAPA SRINIVAS, R PRAKASH RAO, DHARA KALYAN** and **PANDURI VENKATA SAI KUMAR** in partial fulfillment of the requirements for the award of degree of

BACHELOR OF TECHNOLOGY
IN
ELECTRICAL & ELECTRONICS ENGINEERING

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, KAKINADA

During the academic year

2020-2021

Internal Guide
Mr. U Anjaiah
Assistant. Professor
Dept. of Electrical & Electronics Engg.
Narsipatnam.

Dr. T Srinivasa Rao
Professor & HOD
Dept. of Electrical & Electronics Engg.
Avanthi Institute of Engg. & Tech. AIET,
Narsipatnam.

ABSTRACT

The project mainly focuses on the comparison of cascade H-bridge multilevel inverter with THD analysis. The main objective of our project is to increase number of levels i.e. 5-level, 7-level and 9-level with a low THD and sources at the output without adding any complexity to the power circuit. The main advantage of this topology is to reduce the Total Harmonic Distortion (THD), lower electromagnetic interference generation and achieve high output voltage. The Pulse Width Modulation technique has proposed which can minimize the total harmonic distortion and enhances the output voltages from proposed work of five level, seven level and nine level inverter. The operation of single-phase five level, seven level & nine level cascaded H-bridge multilevel inverters are being analysed in this project. The comparison of performances of these two topologies will be discussed on the basis of various parameters such as voltage levels, number of switches, THD level and output. Gating signals for these MOSFET have been generated by comparators. In order to maintain the different voltage levels at appropriate interval, the conduction time intervals of MOSFETS have been maintained by controlling the pulse width of gating pulses (by varying the reference signal magnitude by the comparator). The results of hardware are compared with simulation result. Simulation model (designed in SIMULINK) have developed up to seven level and THD in all the cases have identified.